

# Wafer Dicing Using Dry Etching on Standard Tapes and Frames

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## Abstract

To meet the changing demands of consumer product form factors, there has been a steady shift to thinner and smaller semiconductor die, both of which increase the challenges for die singulation. The traditional approach of saw dicing is facing new limitations due to die damage and throughput. Compounding these issues is the finite width of saw blades, saw blade loading from clearing multiple materials, and orthogonal layout restrictions. Laser dicing has been introduced to address some of these issues, but faces other limitations such as damage from the heat affected zone, ablation residues, throughput, and material incompatibilities (changes in transparency and absorption in the street). In some cases, a combination of both saw and laser has been utilized to surmount some of the technical obstacles.

The recently introduced approach of front-side plasma singulation circumvents many of the limitations of saws and lasers. The technology presented in this work uses standard dicing tape and frames, is through-wafer complete die separation, and does not involve a subsequent wafer thinning or die cleaving step. Our approach utilizes lithographically defined singulation lines with typical widths of 10-15 $\mu\text{m}$ , and delivers chip/crack-free edges with low-stress rounded corners. The parallel nature of this singulation method enables non-orthogonal and non-linear singulation streets allowing die layout and design flexibility not achievable by saws and/or lasers. As a consequence, plasma singulation produces increased good die per wafer through better wafer area utilization, lower die failure (reduced corner stress with rounded geometry), and flexibility in die placement near wafer edge on larger die. One of the unique advantages is that this technology can be implemented without addition of any new masking layers but instead the use of the existing passivation, metals and/or upper dielectrics as masks.

Implementing this technology across a wide range of die applications such as power, memory, logic, imaging sensors, LEDs, and MEMS must address a diverse range of variables such as compatible materials, bond pads/bumps, and backmetal. For dies with backside metal, a non-etch based method to allow full die separation while the dies are still attached to tape has been demonstrated.

## Key words

plasma dicing, die singulation, thin wafers, wafer layout, dicing tape, saw, laser, die strength, yield

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## I. Introduction

Manufacturing in semiconductor and optoelectronics is consistently challenged to reduce fabrication costs and improve device performance. This focus on reducing manufacturing costs is reflected with an emphasis on increasing production yields per wafer and enhanced throughputs. Yield is best defined as the number of good die per wafer that is a result of better utilization of available wafer area and/or fewer die that fail qualification standards.

One way of increasing the quantity of die per wafer is take advantage of the non-negligible area primarily used to separate die, i.e. streets or scribe lines. Typical widths for this purpose are in the 50 $\mu\text{m}$  to 100 $\mu\text{m}$  range depending on the application. The streets are sometimes used for process control monitoring structures (PCMs) but there are process flows with the technology described in this work that still allows significant production advantages. This work describes technology that reduces street widths significantly and consequently allows more area to be used for additional die.

The second way to enhance yield requires improving the structural integrity of the die themselves. By eliminating processes that weaken the die structure from cracking will naturally improve the yield. The use of plasma-based etching to singulate die avoids defects introduced by the current methods of saws and lasers.

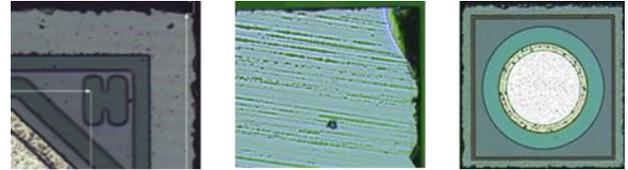
The semiconductor industry has been steadily trending towards thinner wafers primarily to satisfy the consumer product demand for smaller form factors. In addition, there are specific advantages in terms of thermal management and electrical performance that contribute to this trend. Today, wafer processing of  $\sim 200\mu\text{m}$  wafers is common and by 2017, it is estimated that approximately three-fourths of all wafers will be less than  $100\mu\text{m}$  with a significant fraction at “ultra-thin” dimensions of less than  $50\mu\text{m}$  [1]. The established technology of saws and the newer methods using lasers are encountering significant challenges at these wafer dimensions.

This new plasma-based, singulation technology [2] overcomes some of the significant manufacturing challenges encountered in processing thin wafers by conventional wafer dicing technologies. A review of conventional die singulation methods is given in the next section. In the remaining sections, we present the plasma-based die singulation technology and discuss the performance and capabilities, including some added benefits gained by adoption of the technique.

## II. Die Singulation

### (A) Established Technologies: Saws, Lasers

Following wafer level processing, the die must be separated prior to pick-and-place and the final packaging steps. Traditionally the die are separated either by a scribe and break method, mechanical sawing, laser dicing or a combination of these techniques. All three methods rely on a serial or sequential process to cut each and every street on the wafer. As expected, smaller die dimensions generate longer processing times per wafer. If wafer thicknesses decrease, these methods encounter other obstacles to productivity. The scribe and break method relies on careful crystallographic alignment, produces significant particles, and potentially micro-cracking that can impact die strength. Mechanical sawing also induces micro-cracking and delamination, as well as suffers from a reduction in the linear cutting speed as the wafers become thinner. Figure 1 provides typical optical images of dies edges generated by mechanical saws.

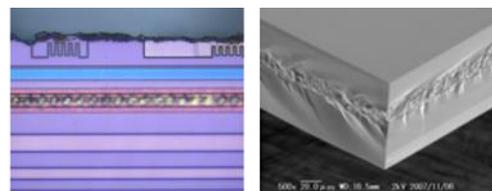


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**Figure 1:** Examples of die edges resulting from mechanical saw dicing (die size  $\sim 220 \times 220 \mu\text{m}$ )

Streets widths must accommodate the finite saw widths and designers often include “seal rings” to prevent possible crack propagation and delamination issues. Significant efforts are made to reduce blade wobble as the blades become thinner which also limits reductions in street widths. Additional issues affecting dicing of many advanced devices have challenged saws with a variety of materials that are not particularly saw compatible, e.g. metals and metal oxides. Nevertheless, the relatively low cost of mechanical saws and their success with thicker wafers has resulted in extensive acceptance.

Recently dicing with lasers has emerged as an alternative to mechanical saws for thin wafers but as illustrated in Figure 2 there are still problems with damage. With the advent of high power pulsed lasers there was an effort to use laser ablation to remove street materials. Although adjustments can be made to address material redeposition issues with protective layers and thermal damage can be reduced, it has not been widely adopted as a standalone solution. Sub-surface laser dicing techniques, also often referred to as stealth dicing where the laser is focused deep in the wafer can potentially allow narrower streets but there is still the issue of a heat affected zone (HAZ) that again limits the amount of street area that can be kept for devices.



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**Figure 2:** Examples of die edges resulting from laser ablation (left) and sub-surface dicing (right).

The local heating creates the potential for interlayer mixing to occur, and multi-layer delamination by thermal mismatch. Consequently, designers include wider streets to protect the die edges from the thermal damage. The growing range of materials found in the streets is also introducing new challenges for the laser processing. Laser dicing is gaining acceptance for applications with fragile substrates commonly found in compound semiconductor devices such as sapphire,  $\text{LiNbO}_3$ , GaAs, and SiC.

Often in CMOS type device wafers, a combination of multiple laser ablation and mechanical sawing passes is used to address the various materials in the streets. This approach to singulate a wafer can seriously impact throughput.

Due to the chemical nature of the process used in the plasma-based singulation technique, no mechanical force or vibration is caused to the wafer thus eliminating wafer breakage, layer delamination, and lateral damage or chipping of the die. There is also no associated thermal-induced damage with the plasma-based technique.

### (B) Plasma-based Die Singulation Technology

This technology is based on multi-step deep reactive ion etching technique developed in the 1990s for silicon based MEMS devices. The technique is commonly referred to as the “Bosch”, DRIE, or DSE™ process, is capable of achieving very deep and narrow trenches in silicon with high selectivity to common mask materials such as photoresist, polyimides, and silicon dioxide. It is now widely accepted and used for through-wafer vias and other packaging applications such as the Shellcase process for imagers.

A newly designed production system for plasma dicing of wafers on tape frames has been developed at Plasma-Therm LLC based on an adaptation of the “Bosch” technique. The system, a MDS™ Micro Die Singulator is fully automated with a dual cassette tape frame loading station and robotic handler. Following the same procedures as for conventional die singulation, prior to processing the wafers are mounted on tape frames. Wafers sizes up to 300mm can be accommodated on each tape frame. To maintain downstream compatibility with existing packaging work flows, the form factor of the tape frames used follows industry standards. Both from a logistics and a cost perspective, this is extremely important when introducing a new technology into an existing manufacturing process line.

The etch reactor module on the system is equipped with an inductively coupled plasma (ICP) source and RF-biased lower electrode. During processing the wafer and tape frame are clamped and cooled. Process gases SF<sub>6</sub> and C<sub>4</sub>F<sub>8</sub> are used in the time-multiplex alternating etching/deposition cycles to etch the silicon in the streets and fully singulate all the die all the way down to the tape.

The system has been specially engineered to handle the tape and avoid degradation during plasma etching. Process termination, when complete wafer dicing has occurred, is achieved by optical endpoint.

Process development has been done on a wide variety of wafer sizes (25 to 200mm) of differing thicknesses from 100 to 700μm, mask materials, die size, and street widths

on the MDS machine. The experimental and model calculation results presented in the next sections are based on this work.

## III. Performance and Capabilities

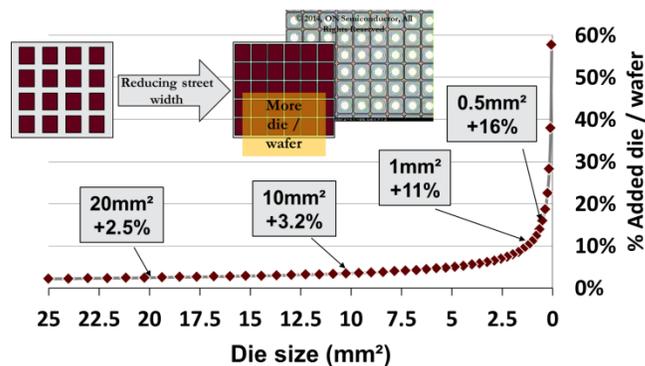
### A. Increase in Die Density

Utilizing wafer real estate by narrowing street widths enables increases in the number of die per wafer. The equation below can be used to estimate the increase [3].

$$DPW = \frac{\pi}{4} \left( \frac{D}{d+w} \right)^2 - \frac{\pi}{\sqrt{2}} \left( \frac{D}{d+w} \right) \quad (1)$$

DPW is the good die per wafer, D is the useable diameter of the wafer, d is the width of the square die, and w is the width of the streets surrounding the die. The number of test die will reduce the number of available good die estimated from equation (1).

We can use this equation to calculate the percentage gain in good die for a particular reduction in street widths for a range of common die sizes from 2mm x 2mm down to 125μm x 125μm. Presented in Figure 3 are calculated results for a 200mm wafer with 3mm edge exclusion and a reduction in street widths from 75μm to 15μm. There is a gain in the number of die per wafer of approximately 11% for a 1mm x 1mm die. This gain increases dramatically as the die size is further reduced.



**Figure 3:** Calculated percentage increase in available complete good die through reduction of street widths from 75μm to 15μm for indicated different square die dimensions.

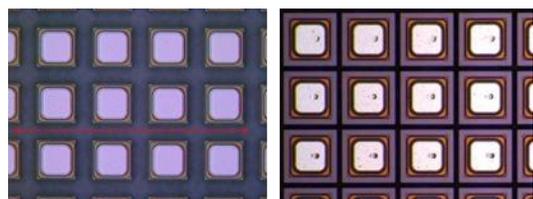
The calculations above are based on a street width of 15μm. However, with plasma-based singulation technology narrower street widths down to 5μm or less are possible as they are lithographically defined. Increasing the aspect ratio of the singulated streets (i.e. wafer thickness divided by the street width) will affect the etch rate but is relatively constant below an aspect ratio of 10:1. The pick-and-place

and tape expansion processes determine the practical street widths and values between 10 and 15 $\mu\text{m}$  are typically used with no change required to current grip ring post dicing expansion parameters.

### B. Increased Die Active Area

The previous example primarily focused on the die density increases for small die when the street widths are reduced. An alternative perspective is to consider the additional die real estate gained while maintaining the same number of die. This increase in active area can be beneficial to device performance. As an example, for power devices, the increased active area leads to a highly desirable reduction in ON resistance.

Figure 4 shows a comparative example to illustrate gain in die size between identical die when the street width is reduced from 90 to 15 $\mu\text{m}$ . In both cases, plasma-based singulation was used.



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**Figure 4:** Plasma-singulated die separated by 90 $\mu\text{m}$  streets image (left) and 15 $\mu\text{m}$  streets image (right).

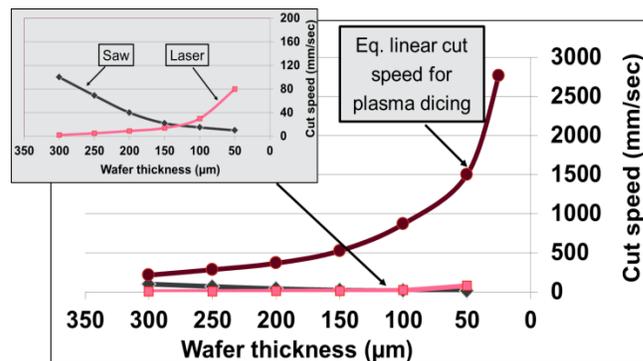
As a point of reference, for a 1mm x 1mm die, reducing the street width from 75 $\mu\text{m}$  to 15 $\mu\text{m}$  increases the die area by 16%. This is particularly relevant when a package limits die size.

### C: Productivity: Throughput

The plasma-based etching for singulation discussed in this work is fundamentally different from the conventional approaches. As mentioned earlier, both mechanical saws and lasers dice a wafer serially or sequentially while plasma-based operates on the streets in a parallel or simultaneous mode.

One metric that can be used to compare the process speeds of various techniques is to generate “effective” or “equivalent” linear cut speeds. For saws and lasers this is simply the linear motion rates. Typically for wafers less than 300 $\mu\text{m}$  thick the rates are in the range of 100 to 200mm/s per pass. Under some circumstances these rates can be increased by a factor of two or three. Figure 5 shows the behavior of these technologies as a function of wafer thickness. Saws are capable of higher linear rates on thicker wafers in contrast to lasers which increase their linear cutting rate as the wafer thickness decreases. Both saws and

lasers have significant obstacles to increase speed for wafers approaching the 50 $\mu\text{m}$  range.



**Figure 5:** Effective die singulation speeds for mechanical saws, lasers, and plasma singulation method *versus* wafer thickness (Plasma data based on 200mm wafer, 15 $\mu\text{m}$  streets and 1mm x 1mm die).

Figure 5 includes equivalent cutting linear speed data for plasma etching. To calculate an equivalent cutting speed it was assumed 1mm x 1mm die with 15 $\mu\text{m}$  streets. Since all streets are cut simultaneously, the equivalent linear rate is simply the summation of all streets divided by the process time. For this comparison, only the actual dicing operation is considered and additional associated steps related to saws, lasers or plasma dicing are not included. For example, processing times for seal rings, protective coatings, multiple cutting passes, or rinsing/cleaning steps are not incorporated in this calculation.

For wafer thicknesses up to 300 $\mu\text{m}$ , plasma street etching provides faster equivalent linear speeds. At the thinner wafer thicknesses the increase is significant and be nearly an order of magnitude greater with plasma etching. Perhaps of even more significance is that the plasma-based technology is not limited at the ultra-thin wafer thickness implementation node.

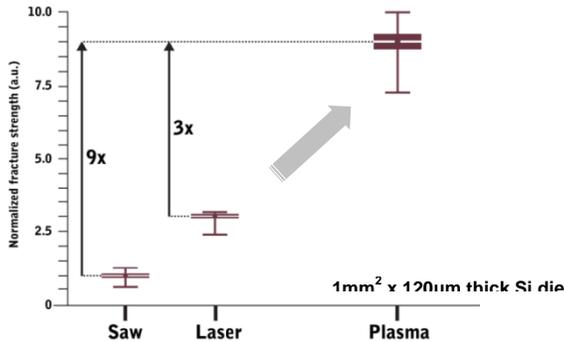
Thus, from a productivity perspective there are potential enhancements from both the addition of new die due to the increased availability of street real estate that was previous discarded and from the actual process time contributing to larger wafers per month production.

### D: Enhanced Die Fracture Strength

The non-physical mechanism of plasma dicing coupled with the lithographically defined street edges offer the potential for crack-free die boundaries. Crack propagation along a surface is often implicated in die failure due to either catastrophic fracturing or a compromise of die function. The actual phenomenon of crack propagation can occur either immediately after its generation or more insidiously at a later time [4]. The fragile nature of most

semiconductor materials, including silicon, makes this phenomenon particularly important. The trend to thinner wafers creates an even greater sensitivity to this destructive mechanism.

Figure 6 provides supporting data comparing the measured relative die fracture strength for singulated 1mm x 1mm die obtained on 120µm thick silicon for mechanical saw, stealth laser, and plasma-based dicing. Four-point bending metrology was used for this data.



**Figure 6:** Die fracture strength comparison between saw, laser, and plasma dicing.

In this example, the plasma-based technique is nearly an order of magnitude more resistant to fracture than dies produced with a mechanical saw, and about three times stronger than those made with a stealth-based laser technique. Porter and Berfield also report improved die strength with the plasma approach compared to traditional mechanical saw [5]. The absence of cracking and chipping in plasma etched die can be seen in the images presented in Figure 7.



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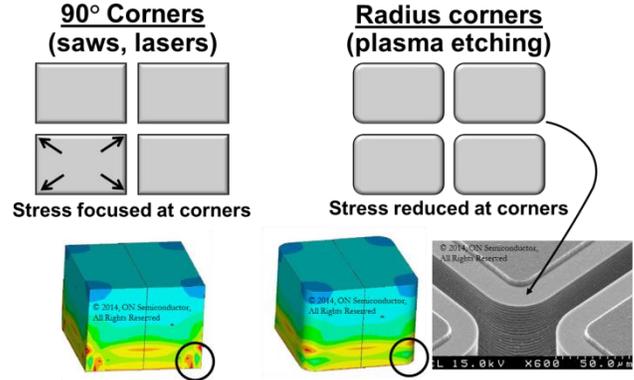
**Figure 7:** Optical pictures (left, center) and SEM (right) showing plasma etched die edge without chipping.

From a technology road map perspective, these results are encouraging as they suggest that plasma dicing can potentially enable even further die thinning versus the incumbent dicing methods.

### E. Reduced Die Stress

Die shape is traditionally based on an orthogonal layout involving 90° corners. Modeling suggests that there is some localization of stress in the corners of dies. This can lead to die failure through fracturing, affect device performance, and create issues for packaging with die having bowing at

the corners. Large, ultra-thin die are particularly affected. Figure 8 illustrates the issue.



**Figure 8:** Stress phenomenon associated with die shape. SEM image of plasma etched die with rounded corners (lower right).

Although the radius corners are primarily attractive for the ability to reduce stress, they have ability to improve other aspects of packaging. One example is to utilize radius corners in applications requiring hermetically metal sealed packages where the corners are traditionally radius machined or need to be drilled out to fit a die with 90° corners.

### F: Non-Orthogonal Die Capability

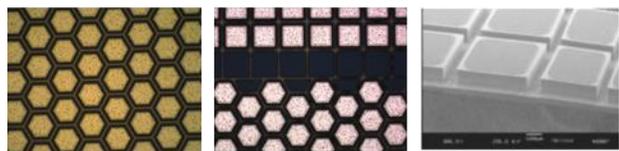
The simultaneous opening of all streets opens some interesting possibilities for controlling die shapes and layout. The majority of die singulated by conventional techniques is either square or rectangular in format and orthogonally aligned on the wafer. With plasma-based singulation, any type of die shape is essentially possible e.g. hexagons and round die. This opens up new possibilities for creative designers for many different device types in electronic, optical, and optoelectronic applications, including the repositioning of large die on the same wafer to optimize the active silicon utilization.

Figure 9 presents a patterned 100mm wafer on dicing tape (left). Individual, fully plasma singulated devices with through wafer holes (right). (Courtesy Opto Diode an ITW company).



**Figure 9:** 100mm patterned wafer on dicing tape (left). Individual, fully plasma singulated devices with through wafer holes (right). (Courtesy Opto Diode an ITW company).

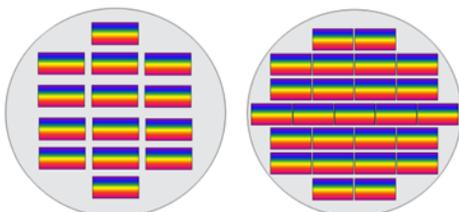
Figure 10 shows additional examples of non-orthogonal die including multi-shaped die on the same wafer produced by the plasma-based singulation technique.



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**Figure 10:** Hexagonal die (left), multi-die shapes (center, right) produced by plasma-based singulation.

Adjusting layout of large die becomes a possibility that can result in large increases in die per wafer. In Figure 11, a rough layout of CMOS imagers illustrates dies prior and after layout re-taping on 300mm wafers taking advantage of single die per reticle helping to offset the die and add more parts per wafer.



**Figure 11:** Layout changes resulting in 11 more die per 300mm wafer (dies 55mm x 35mm).

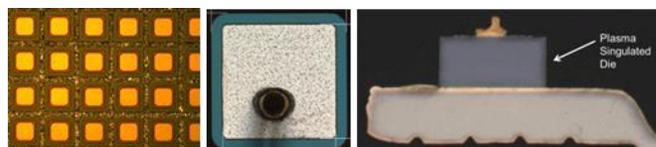
### G: Packing Approaches

There are a wide range of packaging approaches and in this section, we will briefly look at two: wire bonding and wafer level packaging (WLP)/flipchip (with solder bumps). Also, in this section die using backmetal will be described.

#### i. Wire Bonding:

In case of wire bond products, the last front end process step consists in depositing the upper passivation layer (usually a  $\text{SiO}_2 + \text{SiN}$  layer) and etching this material to expose the metal pads (e.g. Al). The wafer is then eventually thinned and mounted on dicing tape frame for singulation with saw and/or laser.

The plasma dicing approach consists of creating a triple passivation layer (existing  $\text{SiO}_2 + \text{SiN} + \text{thin top SiO}_2$ ) and including the street design in the pad mask so that the etch of the passivation takes place both at the pad and street locations. The wafer then follows the exact same process flow as with saw or laser (wafer thinning if desired, mounting on dicing tape frame, plasma dicing). Figure 12 shows the implementation of the plasma-based dicing to working die.



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**Figure 12:** Plasma singulated wafer prior to wire bond assembly (left). Wire bonded die (center). Side view of wire bonded die (right).

#### ii. Wafer Level Bonding/Flipchip (solder bumps)

Similarly to the wire bond assembly approach, the wafer is singulated by plasma dicing using the polyimide or PBO (or any other dielectric used as the upper redistribution layer (RDL) under bump). In that case, after plasma dicing, a DI rinse post clean could be required to eliminate a very soluble stannous fluoride residue resulting from the reaction of Sn with F-based etching gas.

In Figure 13, test wafers (200mm) were re-passivated with Spheron™ dielectric and sputtered with Al/Ni(V)/Cu top metal. The test wafers were then background to  $100\mu\text{m}$  and mounted on standard dicing rings using an industry standard dicing tape. The re-passivated Spheron™ and top metal layer was used as the masking layer for the through wafer plasma dicing to the dicing tape ( $10\mu\text{m}$  wide streets,  $100\mu\text{m}$  thick wafer). With this approach the plasma dicing technology could then be inserted seamlessly into a typical saw or laser singulation process flow without requiring the subsequent removal of the masking layer. This evaluation proved to be very successful with the addition of 10 to 15% more die per wafer.



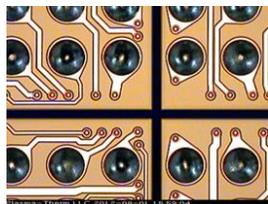
**Figure 13:** SEM image of plasma diced chips showing contact pads with bonding metal.

SEM analysis showed no damage to the top metal layer or to the Spheron™ dielectric layer during the plasma dicing process. The surface of the die was clean and ready for pick-and-place (this due to the plasma clean step performed post plasma dicing within the same tool).

One consideration in using this re-passivated dielectric layer approach to mask the plasma dicing is the reactive ion etch selectivity of silicon to that material. Typically the selectivity will range between 100-300 to 1 depending on the material and the aspect ratio of the street width and Si thickness. The surface condition of the dielectric layer following plasma dicing examined with SEM showed a

typical surface roughness of the dielectric layer similar to the roughness produced during a standard plasma clean process. The plasma dicing process produced consistently uniform non-chipped die edges and corners. There was also no sign of proximity heat damage.

In an alternative process flow, solder bumps already attached to the die can be exposed during the plasma dicing step. This is shown in Figure 14 shows a fully bumped dies that have been plasma diced on tape.

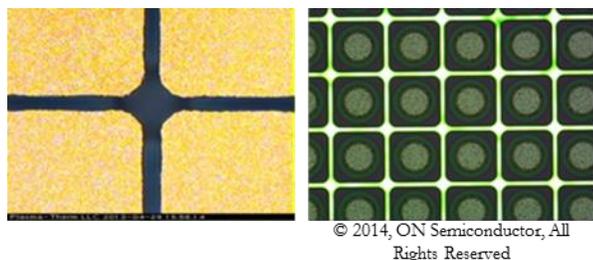


**Figure 14:** Plasma singulated die prior to flip chip or WLP.

### iii. Die with Backmetal

Many devices are currently using backmetal to enhance their performance. Applications include backside metal for power chips and LEDs to serve contacts and for thermal management. Thicknesses of backmetal range from as thin as a few 1000Å to several microns and involve many metallization stacks.

The singulation etch is selective toward most metals and will stop at backmetal layers. If backmetal is thin ( $< 1\mu\text{m}$ ), the die can potentially be picked directly, leaving the backmetal between die on the tape. For thicker backmetals or die that require tape stretch to further separate the die, the backmetal in the singulation openings must be cleared or separated prior to die pick. Techniques have been developed to successfully remove the backmetal between the die. Figure 15 provides two examples with the metal removed.



**Figure 15:** Images showing complete removal of metal from between die. Backside image (left), frontside image (right).

## IV. Conclusions

The recent introduction of through wafer plasma dicing on standard dicing tape is being adopted to provide semiconductor device manufacturing a significant

productivity benefit. This productivity is achieved through several aspects that may include more die per wafer, high yields of good die and flexibility of design without constraints on die shapes, and reduced process times.

Multiple types of devices singulated using the plasma-based technique have been qualified. Completed electrical testing on both product and PCM test structures show no significant shift in electrical performance.

A very important aspect of this technology is the ability to singulate wafers on conventional dicing tape frames. This simplifies implementation and integration into existing process work flows.

## Acknowledgments

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