

# MEMS and Sensors Whitepaper Series



## Current Trends with DRIE/DSE™ Processing for MEMS Devices and Structures

September 2012

**Whitepaper Topics:** MEMS, sensors, DRIE, DSE, Bosch process, dry etching, plasma etching, fab process equipment, 3D silicon structures, SOI, TSVs.

**About Us:** Plasma-Therm is a U.S. based manufacturer of etch and thin film deposition equipment for a number of global compound semiconductor and related specialty markets. For more than 35 years, we have enabled various process technologies by coupling reliable platforms with award-winning service. Plasma-Therm holds over 24 patents for innovation in plasma process technologies, spanning photomask and silicon-based solutions, particularly in relation to deep silicon etch for MEMS applications. For more information, please visit [www.plasmatherm.com](http://www.plasmatherm.com).

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## Introduction

Led by the emerging consumer market, the MEMS industry has experienced a tremendous windfall after recovering from the global economic recession. In 2010, the MEMS market grew by twenty percent with an expected continued annual double-digit growth through 2015. Higher demands in consumer, industrial, medical, automotive, biomedical and other applications, the MEMS market is outperforming the overall semiconductor market by at least a factor of two. This growth is fuelling the need for more sophisticated, more efficient and higher performance processing equipment, and in particular, plasma etching systems used for out-of-plane structures, such as through-silicon vias (TSVs) and other features for MEMS devices. Deep Reactive Ion Etching (DRIE) or Deep Silicon Etching (DSE™) is an industry-leading technology for creating high aspect ratio features in silicon for MEMS and nanotechnology applications. DSE is a type of anisotropic etching technique that etches silicon indiscriminately with regards to the crystal planes, creating deep straight, trenches, and high aspect ratio side walls with excellent depth uniformity.

The most common DSE method, also known as the Bosch DRIE process, is a time-multiplexed anisotropic etching technique with alternating processing steps of passivation deposition and isotropic etching. A polymer-based passivation layer is deposited to selectively protect the surface of the substrate during the etching, preventing lateral etching of side structures. During the etch step, plasma enhanced etching is used to remove material i.e. silicon to define 3D micro-structures. The sequence is repeated, with each cycle removing a small portion at the bottom of the etched trenches or cavities until the desired depth is reached. Due to the repetitive nature of the process, the sidewalls of the vertical profiles typically become scalloped. This and other common limitations of the DSE process have been greatly improved by Plasma-Therm's Versaline® DSE system.

Incorporated in 1975, Plasma-Therm has a long history of industry excellence emerging as a leading supplier of plasma process equipment. Through experience and innovation, Plasma-Therm has developed and incorporated a range of key features in their Versaline® platform, including a host of patented processing technologies. The Versaline® DSE boasts high mask selectivity, low SOI notching and very fast process switching between the passivation and etching steps used to control scalloping effects. Other world-class processing equipment available as part of the Plasma-Therm Versaline® platform include the Versaline® ICP, the Versaline® RIE, the Versaline® PECVD and the Versaline® HDPCVD.

## DSE Process Overview

Plasma Etching or Dry Etching is a plasma based process that facilitates the removal of material from the surface of a substrate. Plasma-Therm has a unique three step process allowing optimization of passivation removal and the isotropic etch step. Competing products commonly uses two process steps; one for passivation and one for the combination passivation and isotropic etch. Since the passivation removal and isotropic etch are coupled together it is challenging to optimize both

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independently. This lack of decoupling is penalized with poorer etch selectivity. In comparison, a three step process can potentially have higher etch rate, allowing less polymer to be produced and increase the mean-time between cleaning (MTBC). Typically, plasma processing of semiconductor materials is performed in a vacuum environment. The key to dry etching is the creation of reactive species within the plasma that can react with the material on the substrate with the formation of volatile reaction byproducts. Dry etching processes are often broken into four mechanisms which must be understood for effective etch system design.

- **Formation of active gas species.**

Gas species are activated within the plasma discharge area. These species include ions, electrons and radicals.

- **Transport of the active species to the surface.**

The neutral species are transported to the substrate surface, mainly by diffusion, while the charged species are accelerated to the surface due to the negative bias on the substrate cathode.

- **Reaction at the surface.**

This step can be further split into three sub-steps: the adsorption of the precursors, the surface reaction and desorption of the products. A wide variety of mechanisms occur during each sub step. For example, processes that depend mainly on the energy of the impinging ions are said to have a large physical component. During a chemical etch, activated neutrals react with the substrate independent of their kinetic energy. In practice, most processes have both physical and chemical aspects.

- **Pump down of the reaction products.**

After desorption, the volatile reaction products diffuse back to the bulk plasma. Here they are exhausted by a vacuum pump. The diffusion directions of etchants and reaction products are a result of concentration gradients of both species, in the bulk plasma and at the substrate surface.

## DSE Process Requirements

Successful DSE processing depends on a range of process requirements. Some requirements can be customer specific, such as vertical sidewall smoothness and tapering of a TSV. Others are more universal and attribute to the process stability, efficiency, effectiveness and cost of system ownership.

### DSE Process Requirements | Profile Control, Sidewall Morphology and Etch Rates

The etching uniformity across a wafer, from center to edge, is a critical factor that will directly impact the consistency of the 3D structures being etched. Ideally, the structures in the outer side regions should be identical to the ones in the middle of the wafer. This will ensure high processing yield and low die-to-die variation. The processing uniformity will depend on several factors, such as how the process equipment is configured and optimized for a given wafer size. Whereas some systems are tailored to

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one specific wafer size, the Versaline® DSE can be configured and tuned for wafers ranging from 3” to 8” in diameter.

A common phenomenon of DSE processing is the scalloping of deep trench sidewalls. This is an artifact of the alternating deposition of passivation and etching. Following a passivation step, ions are directed vertically down at the structure. The ions collide and remove the passivated bottom of the trench thereby exposing the substrate to the chemical etchant. Repeating the etching and deposit steps results in many small, incremental etches. A 500 micron thick wafer would need about 100 to 1000 cycles. Longer cycles results in higher etch rate, but more enhanced scalloping. Faster cycle time and particularly faster switching between passivation and etching can improve the smoothness of the sidewalls.

DSE is a single wafer process where the substrates are processed sequentially, one by one. The time for completing one lot is the processing time of a single wafer times the number of wafers in the lot. With deeper trenches of 100s of microns used for TSVs and higher density of features increasing the etch load, the DSE can become a time-consuming and costly fab process. Etch rates are highly dependent on the etch load, but also on the aspect ratio of the features being processed. A comparison chart has been included in Figure 1, which compares typical industry etching rates for various aspect ratios. Any given MEMS device company has an incentive to add as many structures per wafer as possible to leverage economies of scale and the DSE process equipment owner desires faster processing to minimize processing costs and increase the revenue per time unit. The race is on for higher etch rates to increase the efficiency and processing throughput.

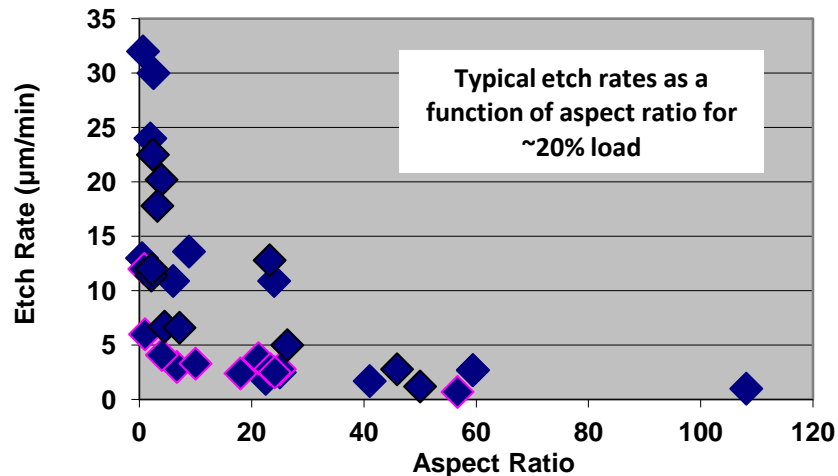


Figure 1 | Typical etch rates for various aspect ratios at ~20% load

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## **DSE Process Requirements | SOI Applications and Endpoint Detection**

DSE is commonly used for etching Silicon-on-insulator (SOI) substrates to create 3D MEMS structures such as TSVs or other features for accelerometers, gyroscopes, microphones, pressure sensors, oscillators and much more. SOI processing uses the top oxide layer to protect areas not to be processed, and a layer of oxide is used as an etch stop layer. SOIs are offered along a wide range of parameters including substrate diameter, thickness, doping levels and oxide thicknesses. Ideally, an SOI structure should be able to have aspect ratio independent vertical structures of varying sizes, shapes and density, with no undercut at the etch entry and notch free. Since DSE processing is CMOS processing compatible; the combination of SOI and DSE is very powerful. It allows making everything from discrete MEMS sensor elements to fully-integrated, monolithic sensor(s) and signal conditioner in one silicon die. In the consumer electronics world, this is especially desirable as market forces and tough competition is aggressively driving higher volumes, better performance and lower unit price in smaller footprint packages.

## **DSE Process Requirements | Stable Process, Reliable Platforms and Easy Maintenance**

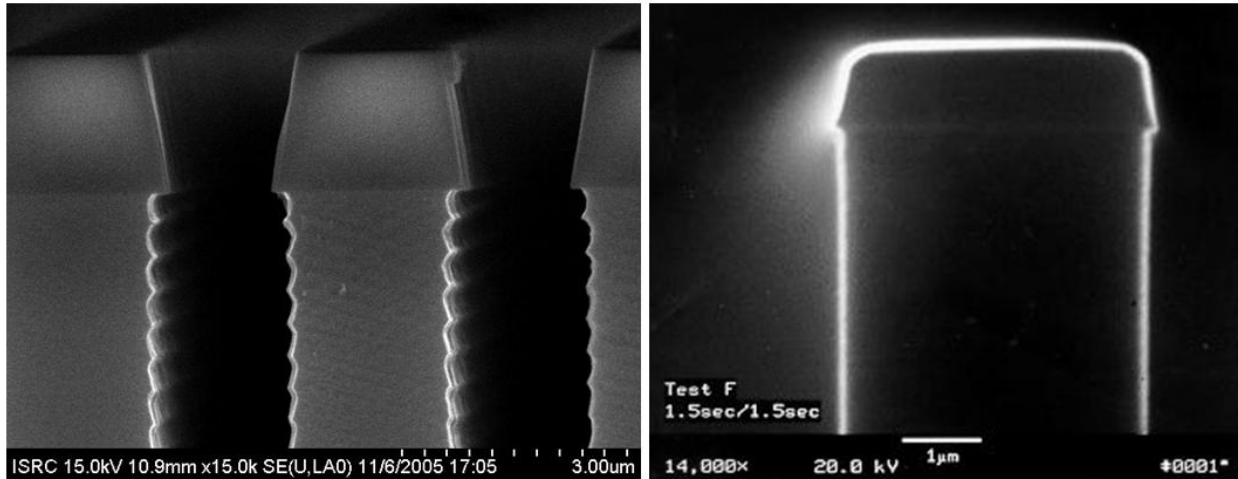
The importance of reliable and stable DSE processing equipment is paramount to successful manufacturing. Above all is the assurance that production recipes produce the same result each and every time it is used for processing a specific substrate type. This relies on monitoring process parameters, but the design and the inherent repeatability of the processing equipment itself is equally important. The more robust and stable a system is the tighter the process control and the associated process control window. This can be an important factor in ensuring that wafers being processed have very little die-to-die, wafer-to-wafer, lot-to-lot, day-to-day and month-to-month variability.

## **DSE Process Tradeoffs and Control**

Plasma-Therm's experience driven DSE systems have a range of features that overcome common drawbacks and limitations of DRIE processing such as scalloping, notching and under etching.

## **DSE Process Tradeoffs and Control | Profile Control, Sidewall Morphology and Etch Rates**

A key feature of the Versaline® DSE is the ability to minimize scalloping of vertical trenches through the use of fast gas switching. Sidewall smoothness is now starting to impact device performance as, for example, the gap in resonators is submicron. Atmospheric devices are impacted as resonance can be affected by flow of air during vibrations. Smoothness can also affect coverage and capacitance (surface area) and field breakdown. The switching time is optimized through a set of dedicated hardware and software to speed up the process to eliminate scalloping effect and other process artifacts commonly associated with other, competitive systems. See Figure 2 below.



**Figure 2 | High aspect ratio trenches, without and with fast gas switching**

Based on controlling process basic parameters such as the power, temperature and pressure, additional metrics including etch rate, sidewall smoothness, mask undercut, SOI notching, Aspect Ratio Dependent Etching (ARDE) and etch selectivity can be controlled. For example, near vertical structures with minimal undercut can be obtained with process morphing™. Process morphing allows process parameters to be automatically adjusted during the etch process to achieve improved profile control. Morph process parameters can be selected and controlled independently. Smooth and automatic changes during processing in combination with process time can be manipulated to achieve customer selected morphing curves with deterministic slopes. For example, the relation between electrode bias, gas, pressure and respective process times can achieve linear or asymptotic, rising and falling, morphing curves.

Plasma-Therm is meeting requirements for increased performance and etch rates by providing higher gas flow and pressure, better gas utilization (See Figure 3) and higher RF power. Increased etch rates will evidently produce more heat at the substrate. This is known as a heat dissipation issue, as the temperature needs to be tightly controlled to ensure uniform and repeatable processing. Excess heat can cause a loss of deposition efficiency potentially leading to non-uniform etching across the wafer as the heat will typically be higher at the middle of the wafer chuck. Plasma-Therm uses a closed-loop controlled cooling chuck (He) to dissipate heat from the wafer during processing.

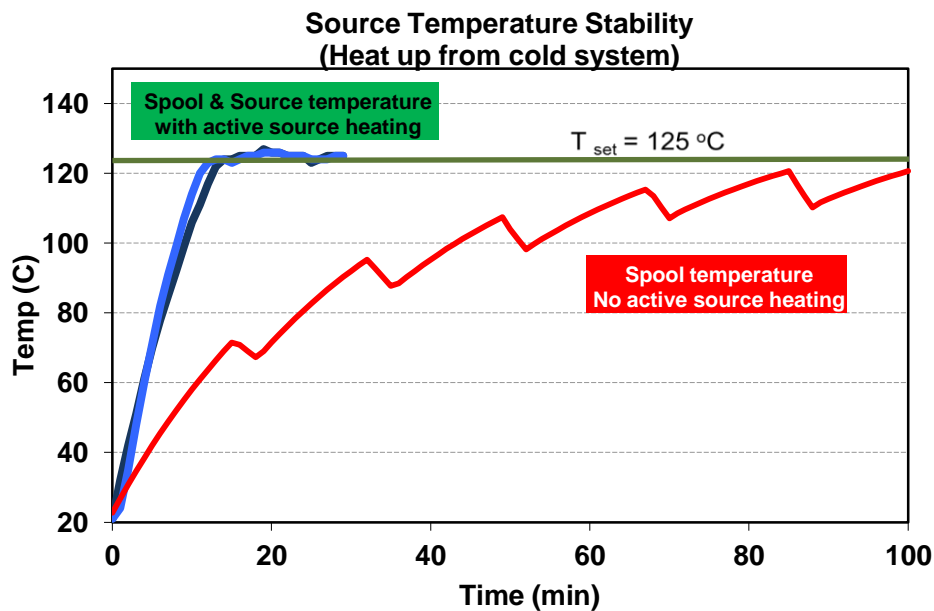
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	Conventional Gas Exchange	Plasma-Therm Fast Gas Switching
Process Cycle Times	Several seconds	<b>Sub-second</b>
Smooth Gas Exchange?	No ( <i>pressure burst</i> )	<b>Yes</b>
Minimizing scallop without losing etch rate?	No (Scallop & etch rate tradeoff)	<b>Yes</b>
Process Limits	MFC response time + gas residence time	<b>Gas residence time</b>

**Figure 3 | Conventional versus Plasma-Therm’s fast gas switching**

Another exclusive feature of the Plasma-Therm DSE system is the use of an active heated source. See Figure 4. The active heating source greatly decreases the time from a cold start to production ready, minimizing equipment down time during maintenance. It also minimizes variation in the source temperature, so wafers receive the same plasma conditions run-after-run and without the typical "first wafer" phenomenon seen with non-actively heated sources. Finally, the mean time between cleaning (MTBC) and maintenance is extended as hardware conditions are optimized with minimized polymer formation in the reactor.



**Figure 4 | Active heating vs. non-active heat source**

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## DSE Process Tradeoffs and Control | SOI Applications and Endpoint Detection

Typical processing of SOI structures result in flaring at the etch stop (oxide) causing notching of the structures and some level of undercutting at the etch entry. Plasma-Therm has a patented technology to control this type of undercutting and notching. The result is almost picture perfect vertical structures as displayed in Figure 5.

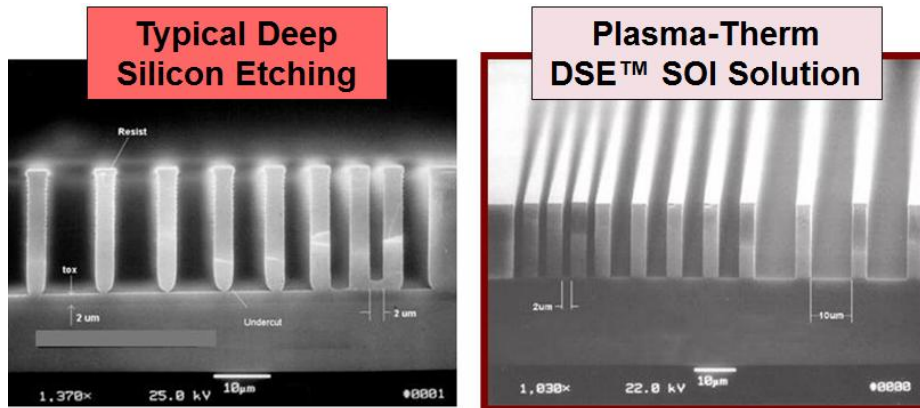


Figure 5 | Plasma-Therm’s DSE process for SOI structures

Higher aspect-ratio structures require lower etching rates to achieve the same processing quality compared to other elements. This effect is known as the aspect ratio dependent etching (ARDE). Bulk micro machined MEMS devices typically include structures with a wide range of feature shapes and sizes. These structures may require different etch rates and, for example, narrow, high aspect ratio trenches may require over-etching to complete the features. Over-etching is particularly undesirable as it is difficult to control and can result in less than optimal 3D structures. Plasma-Therm has developed techniques and process controls to almost eliminate ARDE effects, resulting in more efficient processing, and producing uniform feature depths for ease of design rules.

Etching of SOI wafers often use a silicon oxide layer as an etch stop and a fixed etch time for process control. If the etch proceeds beyond this time, the etchant will start removing the oxide layer and degrade the profile (i.e. notching). Optical emission spectrometry (OES) can be used to detect plasma process termination time by analyzing the light emitted from a plasma source to deduct information about the chemical and physical states. The Versaline® DSE is equipped with an integrated endpoint detection system called OES. This OES consists of a wide range spectrometer employing a CCD array, with real time monitoring and adjustable thresholds. It is highly sensitive making it capable for low load (~0.5%) applications and is proven to increase productivity and quality controlling over etching.

## DSE Process Tradeoffs and Control | Stable Process, Reliable Platforms and Easy Maintenance

Conventional DRIE systems exhibit a “pressure burst” when changing between the passivation deposition and the etching step. Plasma-Therm has developed a smooth pressure transition; the “hold



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and release” pressure control. This feature eliminates pressure bursts and ensures very stable and reproducible run-to-run production results. The hold and release pressure control is a closed loop control algorithm with superior stability and reproducibility compared to more common open loop position pressure control systems.

## Example 1 | Etching SOI

The example in Figure 6 displays a cross-section of a notch-free, vertical SOI feature. The feature is smooth along the side walls all the way down to the bottom of the cavity where the Silicon is opening to oxide. This is highly desirable, especially for MEMS devices where SOI is commonly used in 3D structures.

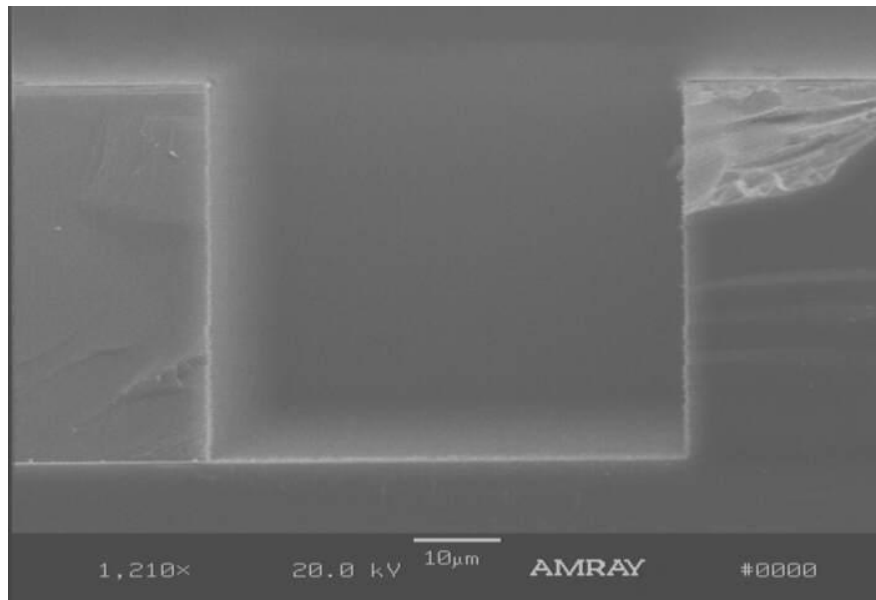
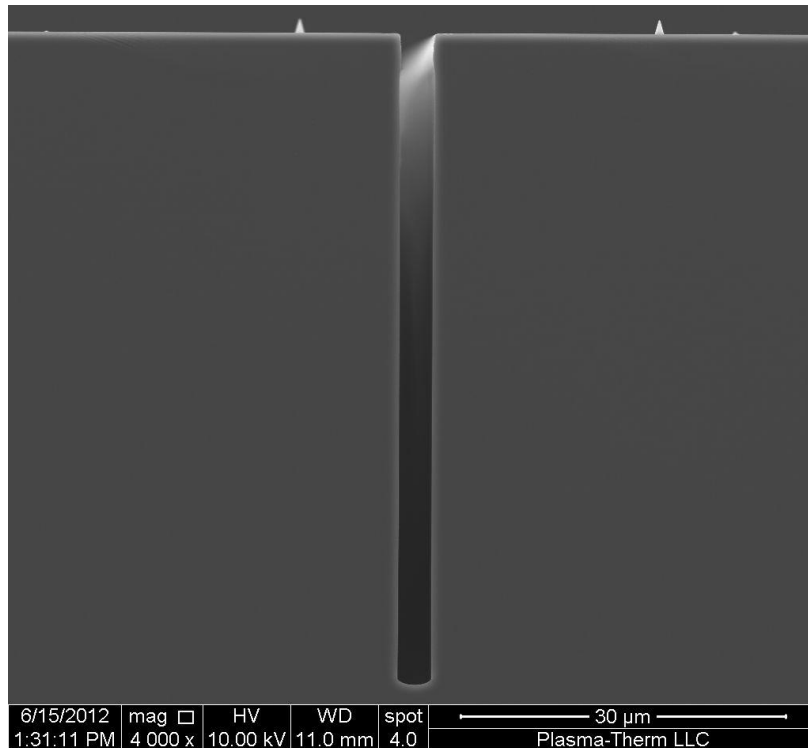


Figure 6 | Notch free SOI

## Example 2 | Sidewall Smoothness of High Aspect Ratio Trenches

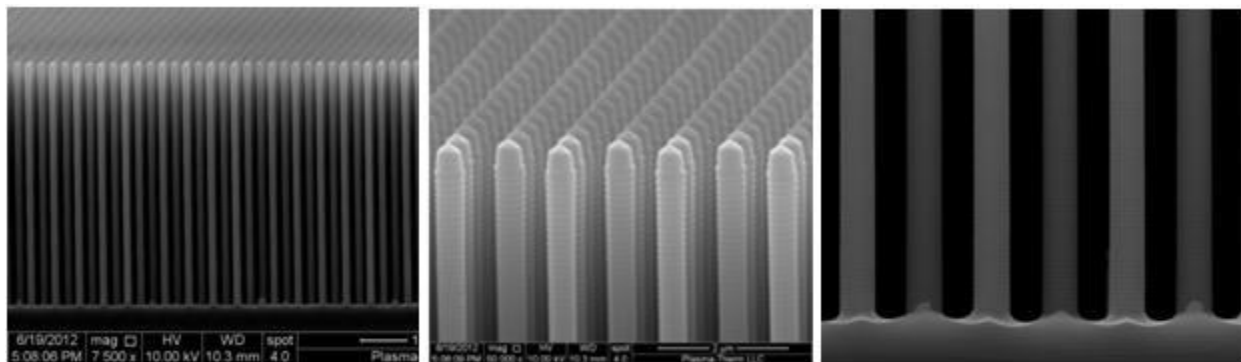
The second example, in Figure 7, is of a high aspect ratio 30:1 trench with very smooth sidewalls and outstanding profile control. Side wall scalloping for this particular feature is less than 20nm. This is a great example of the excellent capabilities of the Plasma-Therm DSE.



**Figure 7 | High aspect ratio**

**Example 3 | “Nano” Etch and Other Unique Structures**

The final example displayed in Figure 8 depicts very small dimensioned nano etch trenches with smooth, vertical sidewalls. The trenches are 500nm wide with 350nm openings, 17μm height and average scalloping of 10nm.



**Figure 8 | DSE nano trenches**

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## Summary and Conclusions

Plasma-Therm is an industry leader in processing equipment that specializes in modular systems with state-of-the-art technology and configuration flexibility. With demonstrated production proficiency in high volume manufacturing environments coupled with a strong presence at many major research institutions, Plasma-Therm has secured a leadership position as a preferred supplier of plasma process equipment. Plasma-Therm's Versaline® DSE system has a range of unique capabilities that makes it an excellent choice for processing SOI wafers for MEMS applications. Key features include patented technology for pressure control, notch-less SOI, fast gas switching and endpoint detection algorithms. Real world examples have been provided to prove the excellent process capabilities for high aspect ratio structures, notch-free SOI and unique nano scale features.

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