Process and Equipment Challenges for MEMS Deep Silicon Etching

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Introduction

The diverse applications comprising MEMS technology require an appropriate suite of processes and equipment. Applications range from microfluidic pumps, to optical switches, to pressure sensors, to three-dimensional chip stacking, to accelerometers, to gyroscopes, to switches, to variable capacitors and inductors. Even this small sampling of devices puts rigorous demands on the process characteristics of etching rates, morphology, profiles, and material selectivities. For example, microfluidic devices and optical switches often have features tens of microns in depth but with sidewall smoothness requirements in the tens of nanometers range. Microactuator and through wafer via applications usually consider silicon etching rate and profile of greater importance. Thus, it is clear that the processes must be flexible to address the multiple research and development needs of the rapidly expanding MEMS market. From a production perspective, tools sets must provide robust and cost effective performance.

One approach employed by equipment suppliers, such as Unaxis Semiconductors, is to provide both low cost-of-entry research and development systems, and systems more suitable for production. It is important that processes can be transferred from the development phase to production with minimal additional process optimization efforts. Where a manual load system with a set of processes intended for device feasibility and prototyping (or even low volume) is an appropriate solution for the laboratory or small facility, a cassette-to-cassette system with an enhanced set of processes is more fitting when volume production and cost-of-ownership are considered. This combination of equipment enables a smooth transfer from innovation to commercialization.

This article presents significant improvements in processes and hardware resulting in enhanced reproducibility and uptime, while fulfilling the demands of throughput, structure profiles, and morphology. More specifically, high etching rates, improved smooth sidewall morphology, endpoint detection with application to silicon-on-insulator (SOI), and process control are discussed.

High Silicon Etching Rate Processing and Profile Control

Silicon etching rate strongly correlates with free fluorine concentration. High values of fluorine radicals are obtained with large SF_6 flow rates and a relatively large coupled power to dissociate the SF_6. Thus, fast etching rate is most economically achieved when

the pumping capability and power supplies are matched to the appropriate application. Silicon etching rates required in the laboratory are often much lower than those needed for production and thus, the equipment configuration and corresponding cost should be considered. It is unfortunate that many etching rate discussions do not take place in the context of the device being fabricated, the needed throughput, or market demands. However, when high rate etching is required, whether it be for production throughput or to avoid unendurable process times in the laboratory, it is usually important to maintain feature profiles without unnecessary tradeoffs to mask undercut or roughness. Table 1 provides some examples of achievable etching rates and depths. Figure 1 shows a 30 µm trench feature with vertical sidewall profiles at ~12 µm/min. Etching rates approaching 20 µm/min can be achieved with larger features. Even higher etching rates are possible when the profile is not a primary consideration.

(Insert Figure 1)

Table 1. Sample etching rates for features of various dimensions.

Feature Dimension	Depth Etched	Etching Rate
2.5 µm trench	15 µm	8 µm/min
30 µm trench	40 µm	12 µm/min
100 µm trench	100 µm	18 µm/min

Figure 1: SEM images test structure feature that is 30 µm wide and 40 µm deep, etched at nearly 12 µm/min. while maintaining vertical sidewall profiles.

The extensive range of feature sizes and aspect ratios has made profile control a challenging issue. One way of handling this diversity is with a technique sometimes referred to as "morphing".[1] With this technique, etching parameters are changed automatically, continuously, and smoothly during processing. By adjusting process variables such as pressure, gas flows, power, and others during etching, the profile can be adjusted to compensate for changes in mass transfer of reagents and products as the features are etched. Figure 2 shows an example where the process has been "morphed" to provide a vertical structure.

(Insert Figure 2)

(a) (b)

Figure 2: Effects of profile control on a free-standing structure. (a) without morphing (b) improved with morphing. The morphed structure avoids the taper seen in the unmorphed feature.

Sidewall Morphology

As aforementioned, there are applications requiring extremely smooth sidewalls, typically those involving fluid dynamics such as micro-mixing chambers or serving an optical function such as photonic switches. Achieving the desired degree of smoothness on a vertical profile while maintaining an acceptable etching rate has proved challenging with traditional deep silicon etching techniques.

The Bosch process, generally accepted for deep silicon etching, results in the formation of "scallops" on the sidewall of etched structures. This manifestation of sidewall roughness is a direct consequence of the alternating deposition and etching cycles. The timing of the steps in each cycle can be directly correlated to etching rate and sidewall roughness. One approach to address the roughness issue is the inclusion of additional gases, such as oxygen or nitrogen, to encourage more anisotropic etching behavior. Though this approach does reduce roughness, it is difficult to control and there is a loss in etching rate.

Another method to improve sidewall roughness utilizes shorter etching cycles. The length of the etching cycle is primarily limited to the relatively slow response of the mass flow controllers (MFCs). Though fast digital MFCs have improved the situation,[2] they may still be limited in their ability to stabilize gas flows and avoid a flow burst at the start of each cycle, either of which will affect process reproducibility and stability. Efforts to reduce the initial gas surge by maintaining a minimal flow rate during the "off" cycle causes process gas flow overlap and have not been successful in producing cycle times of less than two seconds.

Recently, Unaxis Semiconductors developed a proprietary, fast gas switching technique to control gas introduction into the processing chamber and thus, reducing sidewall roughness. This new technique eliminates destabilizing flows, even with very short step cycles and promotes smoother transitions between etching and deposition steps. It is now possible to reduce step times to the limiting value of the gas residence time constants of

the processing module. More rapid etching rates with smoother sidewalls can be achieved by avoiding wait steps for pressure stabilization.

Figure 3 shows the correlation between the frequency of sidewall scallops with etching rate. In conventional Bosch processing the distance between the scallops increases as the etching rate increases. (Due to ease of measurement, the distance between sidewall scallops is used as a useful measure for the depth or amplitude of the scallops.) This figure shows dramatic improvement with the new, fast gas switching technique where increases in etching rates do not increase sidewall roughness. In Figure 4, the results of this method are illustrated with scanning electron microscope (SEM) images. Smooth sidewalls with etching rates of ~7 µm/min are possible with 100 µm wide trenches and etching rates >4.5 µm/min are possible with trenches as small as 2.5 µm wide.

Process step times in the half second regime, limited only by the residence time constant of the module, can be implemented without expensive hardware.

(Insert Figure 3 a & b)

(a) (b)

Figure 3: (a) Defining scallop length and depth, (b) Etching rate for conventional etching and with the new, fast gas switching method where rate and smoothness are achieved.

(Insert Figure 4 a, b & c)

Figure 4: Test structures are used to monitor sidewall smoothness characteristics. (a) SEM image of sidewall scallops created with conventional etching process, (b) SEM image of smoother sidewalls using fast gas switching technique, (c) Sidewall roughness <10 nm (magnification of 80k)

Process Pressure Control

The cyclical nature of deep silicon etching puts unique demands on common methods of pressure control. Typical closed loop pressure control is inadequate as the etching and deposition steps become faster and faster. Throttling valves have difficulty responding to the pressure setpoints of the individual steps and the response lag is reflected in poor pressure control. Reverting to open loop throttle position control solves the problem partially but there tends to be drift during long processes and poor wafer-to-wafer reproducibility as seen in the Figure 5a. It is clear over the process time measured, pressure has drifted considerably and appears to continue to move out of compliance.

In efforts to provide a stable processing environment, Unaxis Semiconductors has developed a proprietary algorithm where this pressure drift can be avoided. Using this new control mode, the pressure data presented in Figure 5b demonstrates its effectiveness at maintaining accurate and stable process pressure.

(Insert Figure 5 a & b)

Figure 5: Laboratory tests with (a) Pressure control using throttle position setpoints shows drift whereas, (b) Pressure control using proprietary Unaxis algorithm combining pressure and throttle position control shows long term pressure stability.

Silicon-on Insulator Endpoint Detection

SOI processes require endpoint detection to avoid the effects of unnecessary over-etching. Aspect ratio dependent etching (ARDE) occurs when etching features of different dimensions. As aspect ratios (feature etching depth divided by width) increase, mass transfer of reagents and etching byproducts in and out of the etched feature becomes limiting. Thus, slower etching of high aspect ratio features compared to low aspect ratio features is observed. This characteristic affects SOI processes because larger features (those with lower aspect ratios) will etch to the oxide insulator layer before the smaller features. During the overetching period, while the larger features "wait" for the smaller features to reach the oxide, the larger features may experience unwanted "notching" at the oxide silicon interface. To counteract this effect, a sensitive method for detecting small amounts of oxide exposed during the etching is needed. With sensitive endpoint detection a switch to an SOI "finish etch" can occur as early in the process as possible. Figure 6 shows a process development pattern used to study endpoint capabilities on SOI wafers. A wide range of aspect ratios can be accommodated with an appropriate endpoint detection technique.

(Insert Figure 6)

Figure 6: SEM image of a SOI test structure showing a wide range of feature widths range from 2.5 um to 100 um wide that result in aspect ratios from approximately 20 down to 0.5.

The cyclical nature of deep silicon etching makes it difficult for the conventional endpoint detection methods of laser reflectance interferometry and optical emission spectroscopy (OES) to be sufficiently sensitive. However, with signal processing methods detection of as little as 2% open oxide areas on 150-mm wafers can be detected. Figure 7 shows an unambiguous endpoint signal that can be extracted from the wide variations of emission intensities from the etching and deposition steps.

(Insert Figure 7)

Figure 7: OES endpoint signal from SOI etching with 2% oxide exposed on 150-mm wafer.

Applying Deep Silicon Etching Technology

Although the well known MEMS applications of inkjet printers, pressure sensors, and airbag deployment accelerometers have demonstrated distinct performance advantages and market penetration, there are also other less well know applications providing success stories. One such example of a non-typical MEMs application is the use of microactuators for effectively increasing performance in Hard Disk Drives (HDD).[3] Seagate Technology has applied a MEMS solution to a problem that required a small device mass, low cost of production, easy integration, which was mechanically and electronically compatible. The resulting design, a microactuator, is made with wafer-level batch fabrication, utilizing bulk silicon micromachining, and includes high aspect ratio structures. With device etching depths ranging from 50 µm to 200 µm, relatively high etching rates are necessary for adequate throughput. Features range from narrow channels that serve to define springs to large areas which accommodate attached device components. Although the range of feature sizes and the requirement that profiles be vertical can be satisfied with morphing, it was not required for this device. A SEM image of the deep silicon etched portion of the microactuator is shown in Figure 8 while Table 2 provides a summary of some of the etching characteristics.

(Insert Figure 8)

Figure 8. Microactuator frame fabricated with Unaxis DSE™ technology

Table 2: Summary of the Unaxis DSE™ II process results optimized for the microactuator application

Parameter	Value	Description
Etching Rate	6.5 um/min	Low aspect ratio features
Within Wafer Uniformity	<2.5 %	(max-min/)2 x average 4" wafer
Selectivity	~600:1	Si: SiO_2
Sidewall Angle	90°±1°	

Conclusion

In this work we have shown results from processes that produce extremely smooth sidewalls with roughness less than 10 nm. This high degree of surface smoothness can be maintained with silicon etching rates in excess of 7 µm/min. Volume production often emphasizes etching rates as a route to lowering costs with increased throughput. Significantly higher rates can be achieved for applications where silicon etching rate and profile are of greater importance than sidewall morphology. However, the increased rates are often accompanied by higher initial capital costs which must be considered in the context of market size and dynamics. Other applications, such as those utilizing SOI processing steps, usually require sensitive endpoint detection methods. A signal processing approach which can provide SiO_2 sensitivity to load areas of 2% on 150-mm wafers has been described in this article.

Moving deep silicon etching from the exploration phase into production requires many issues that go beyond the basic etching process to be addressed. This article focuses on several of these manufacturing issues including high etching rate for throughput, sidewall smoothness for device performance, pressure control for long term process stability and reproducibility, and sensitive endpoint detection for low load conditions. There are always tradeoffs between performance and capital costs and it is important that there is a good match between the process capability needed and production volume. To accommodate performance, volume, and cost needs, vendors are introducing manual load and cassette-to-cassette systems with the appropriate hardware to support desired processes. This article describes recent advances in deep silicon etch processing and system components that encourage MEMS development and commercialization efforts.

Acknowledgements
This article is based on a presentation given at the Commercialization of Micro and Nano Systems Conference (COMS) in 2003.

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