ADVANCES in DEEP SILICON ETCHING

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Introduction

The rapidly expanding MEMS market is in a phase requiring tool sets satisfying research and development needs in addition to flexible, robust, and cost effective production solutions. One approach is to provide a low cost-of-entry research and development system with a set of processes appropriate for device feasibility and prototyping. Cost-of-ownership production solutions are established using a cassette-to-cassette system with an enhanced set of processes tailored for volume production. This combination of equipment enables a smooth transfer of laboratory technology to volume commercialization. In this work we describe recent advances in deep silicon etching which emphasize increased etching rates and improved smooth sidewall morphology. For example, microfluidic devices, chemical, biological and optical transducers can benefit from a new Unaxis approach that forms extremely smooth sidewalls with scalloping less than 35 nm deep. This high degree of surface smoothness can be maintained with a silicon etching rate in excess of 7 µm/min. For other applications, such as pressure and acceleration sensors when silicon etching rate and profile are of greater importance, silicon etching rates of more than 12 µm/min can be obtained. Volume production often emphasizes etching rates as a route to lowering costs through increased throughput. However, the increased rates are often accompanied by higher initial capital costs that must be considered in the context of market size and dynamics. Other applications, such as those utilizing silicon-on-insulator (SOI) processing steps, require sensitive endpoint detection methods. New signal processing approaches that can provide SiO_2 sensitivity to load areas of 2% on 150-mm wafers will be reviewed. Finally, new innovations in long-term process/pressure stability that contribute to transferring MEMS from the laboratory to production will be explained. These advances, when coupled with Unaxis' extensive experience as one of the largest suppliers for production deep silicon etching (DSE), PECVD, and PVD equipment, form a MEMS leading platform and process suite.

Sidewall Morphology

The Bosch process, generally accepted for deep silicon etching, results in the formation of "scallops" on the sidewall of etched structures. This manifestation of sidewall roughness is a direct consequence of the alternating deposition and etching cycles. The timing of the steps in each cycle can be directly correlated to etching rate and sidewall roughness. One approach to address the roughness issue is the inclusion of additional gases, such as oxygen or nitrogen, to encourage more anisotropic etching behavior. Though this approach does reduce roughness, it is difficult to control and there is a loss in etching rate.

Another method to improve sidewall roughness utilizes shorter etching cycles. The length of the etching cycle is primarily limited to the relatively slow response of the mass flow controllers (MFCs). Fast digital MFCs are still limited in their ability to stabilize and there is a flow burst each cycle that affects process reproducibility and stability. Efforts to reduce the initial surge flow by maintaining a minimal flow rate during the "off" cycle has not produced cycle times less than 2 seconds and causes process flow gas overlap.

Recently, we have developed a proprietary fast gas switching technique to control gas introduction into the processing chamber and thus reduce sidewall roughness. This new technique eliminates destabilizing flows even with very short step cycles and promotes smoother transitions between the etching and deposition steps. With this new technique it is possible to reduce step times down to the limiting value of the gas residence time constants of the processing module. By avoiding steps that wait for the pressure to stabilize, more rapid etching rates with smoother sidewalls can be achieved.

Figure 1 below shows the correlation between the frequency of sidewall scallops with etching rate. In conventional Bosch processing the distance between the scallops increases as the etching rate increases. (Because of the ease of measurement we use the distance between

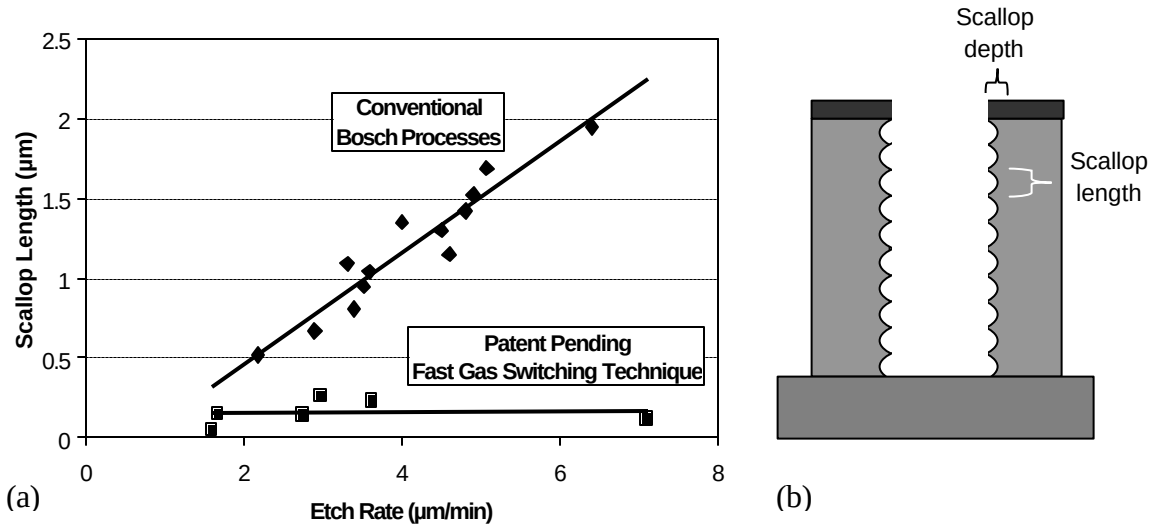

Figure 1: (a) Correlation between scallop length and etching rate with conventional etching processes and the small scallop length possible with high etching rates using new fast gas switching method. (b) scallop depth is related to scallop length.

sidewall scallops as a useful measure for the depth or amplitude of the scallops.) This figure also shows the dramatic improvement with the new fast gas switching technique where increases in etching rates do not increase sidewall roughness. In Figure 2, the results of this method are illustrated with scanning electron microscope (SEM) images.

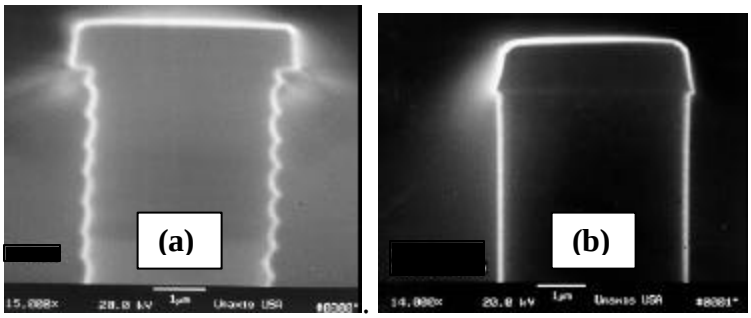

Figure 2: SEM images (a) sidewall scallops using conventional etching process. (b) smoother sidewalls using fast gas switching technique with an etching rate of >7 µm/min. The smoother sidewall with <35 nm roughness is achieved at twice the etching rate in (a).

Fast gas switching can be implemented without expensive hardware that permits step times in the half second regime and is only limited by the residence time constant of the module.

High Silicon Etching Rate Processing

Silicon etching rate is a strong function of fluorine concentration during the etching step. High values of free fluorine are obtained with large SF_6 flow rates and relatively large coupled power to dissociate the SF_6. Thus, fast etching rate is most economically achieved when the pumping capability and power supplies are matched to the appropriate application. It is unfortunate that many etching rate discussions do not take place in the context of needed throughput or market demands. Still it is relevant that high rate etching is possible while maintaining feature profiles without unnecessary tradeoffs to mask undercut or roughness. Table 1 provides some etching rates and etching depths achievable. Figure 3 shows a 30 µm trench feature with vertical sidewall profiles at ~12 µm/min. Etching rates approaching 20 µm/min can be achieved with larger features.

Table 1. Example etching rates for features of various dimensions.

Feature Dimension	Depth Etched	Etching Rate
2.5 µm trench	15 µm	8 µm/min
30 µm trench	40 µm	12 µm/min
100 µm trench	100 µm	18 µm/min

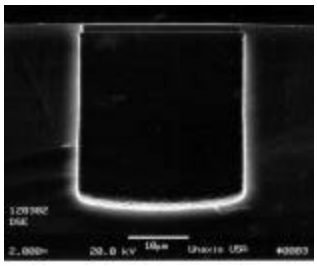

Figure 3: SEM images of a feature 30 µm wide and 40 µm deep that was etched at nearly 12 µm/min.

Process Pressure Control

The cyclical etching process of deep silicon etching puts unique demands on common methods of pressure control. Typical closed loop pressure control is inadequate as the etching and deposition steps become faster and faster. Throttling valves have difficulty responding to the pressure setpoints of the individual steps and the response lag is reflected in poor pressure control. Reverting to open loop throttle position control solves the problem partially but there tends to be drift during long processes and poor wafer-to-wafer reproducibility as seen in the Figure 4a. It is clear that over the process time measured, the pressure has drifted considerably and appears to continue to move out of compliance.

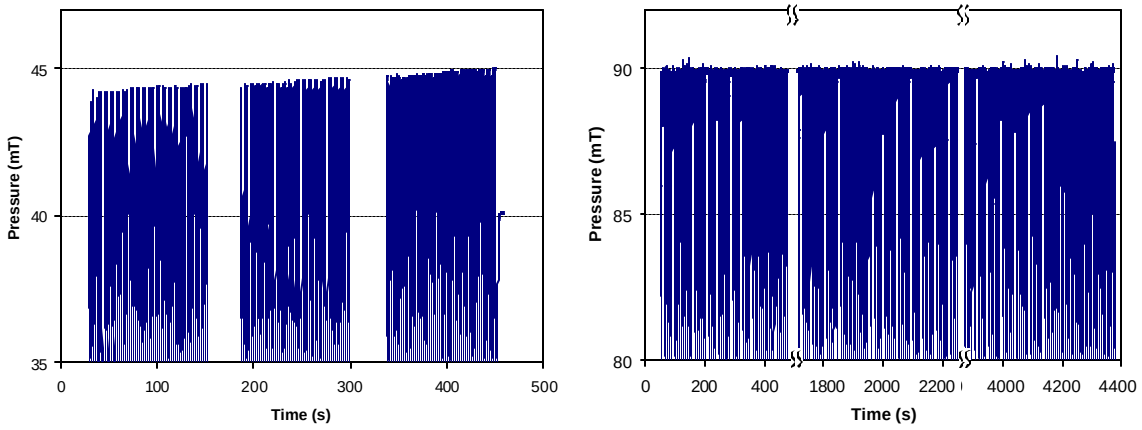

Figure 4: (a) pressure control using throttle position setpoints, (b) pressure control using proprietary algorithm combining pressure and position control.

In efforts to provide a stable processing environment we have developed a proprietary algorithm where this pressure drift can be avoided. The pressure data presented in Figure 4b using this new control mode demonstrates its effectiveness at maintaining accurate and stable process pressure.

Silicon-on Insulator Endpoint Detection

SOI processes require endpoint detection to avoid the effects of unnecessary over-etching. Aspect ratio dependent etching (ARDE) is an inherent phenomenon when etching features with different dimensions. As aspect ratios (feature etching depth divided by width) becomes significant, the ability for mass transfer of reagents and byproducts in and out of the etched feature becomes limiting. Thus, it is common for high aspect ratio features to etch more slowly than low aspect ratio features. This characteristic affects SOI processes because larger features (those with lower aspect ratios) will etch to the oxide insulator layer before the smaller features. During the overetching period while the larger features "wait" for the smaller features to reach the oxide, these larger features may experience unwanted "notching" at the oxide silicon interface. To counter this effect, a sensitive method for detecting when small amounts of an oxide is exposed during the etching is needed so that a switch to a SOI "finish etch" can occur.

The cyclical nature of the deep silicon etching makes it difficult for the conventional endpoint detection methods of laser reflectance interferometry and optical emission spectroscopy (OES) to be sufficiently sensitive. However, through signal processing we are able to detect open oxide areas of <2% on 150-mm wafers. Figure 5 shows an unambiguous endpoint signal that can be extracted from the wide variations of emission intensities from the etching and deposition steps.

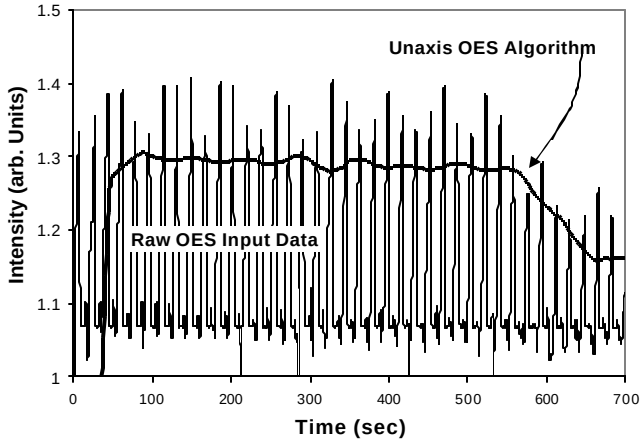

Figure 5: OES endpoint signal from SOI etching with 2% oxide exposed on 150-mm wafer.

Conclusion

For deep silicon etching to move into production from laboratories, start-up companies, and prototyping, there are many issues that go beyond the basic etching process that must be addressed. We have tried to focus on several of these manufacturing issues in this paper: high etching rate for throughput, sidewall smoothness for device performance, pressure control for long term process stability and reproducibility, and sensitive endpoint detection for low load conditions. As might be expected, there are tradeoffs between performance and capital cost and it is important that there is a good match between the process performance needed and production volume. To accommodate performance, volume, and cost needs, vendors are introducing manual load and cassette-to-cassette systems.