Characterization of a 10 μm/min chlorine-based ICP etch process for GaAs vias

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Abstract

The development of a 10μm/min etch process for the definition of backside vias in GaAs is described. GaAs etch rates as high as 15.5μm/min are reported. A designed experiment (DOE) is performed to characterize the effect of ICP power, RIE power, fraction of Cl_2, and pressure on the GaAs etch rate, selectivity to photo-resist and etched via profile. A high chlorine flow rate is used and in this regime it is found that GaAs etch rate is primarily a function of ICP power, indicating that dissociation of Cl_2 to Cl is the rate limiting step. Selectivity to photo resist is found to be only a function of bias power, providing an independent control of via slope when a sloped resist mask is employed. The variation of etch rate with via diameter is also reported.

Introduction

GaAs devices are used extensively in the wireless telecommunications industry, where the high electron mobility of GaAs makes it well suited for high frequency, low noise, high gain applications. Although it has excellent electrical properties, GaAs is a relatively poor thermal conductor, making it difficult to remove heat efficiently from

power devices. A commonly used solution to this issue is the formation of vias from the wafer backside to the frontside circuitry. Such vias provide a good thermal path for heat removal as well as a low impedance ground.

Backside via formation is one of the final steps in the device fabrication. After completion of the frontside processing, the wafer is mounted face down on a carrier wafer and mechanically thinned to a thickness of approximately 100 microns. The back of the wafer is then patterned using photo-resist and the vias are plasma etched through the thinned substrate, stopping on the frontside metal. After resist removal the vias are metallized, typically by sputtering a gold seed layer followed by an electroless gold plating to act as the heat sink / ground connection.

A manufacturable backside via etch process is subject to a number of constraints:

- Short process time – the etch process is required to etch vias 60 microns in diameter by 100 microns deep. A typical via etch at 6 μm/min results in etch times of 17 minutes per wafer.
- High GaAs:Stop Metal etch selectivity – since the thinning process can result in thickness variations of several microns, it is imperative that the via etch process not damage or etch the underlying frontside metal contact
- High GaAs:Resist etch selectivity – the via etch process is typically required to etch through a 100 micron GaAs layer. GaAs:Resist selectivities greater than 10:1 are

necessary to keep the required photoresist thicknesses under 14 microns – the maximum resist thickness typically achievable in a single spin.

- Excellent etch rate uniformity – a highly uniform etch reduces the need for extensive overetches reducing the overall process time
- Result in a via with good electrical properties – in order to achieve good electrical properties, the resultant via must be compatible with the downstream metallization capabilities. Sloping the via profile during the etch process reduces the effective aspect ratio of the via which facilitates metallization
- Robust process – the via etch should be insensitive to upstream (grind & lithography) process variations as well as feed material (substrate type).

Etching of GaAs through wafer vias for backside contact is not a new plasma application. Early work focused on process development in an RIE configuration using primarily CCl_2F_2 [1-3], $SiCl_4/Cl_2$ [4-7] and BCl_3/Cl_2 [8-11] chemistries. While etch rates in excess of 60 μm/min have been reported[12], these high rates were only achieved at elevated temperatures at the expense of undercut feature profiles and poor etch rate uniformity. In order to achieve the profiles and uniformity required in a production environment, manufacturable RIE processes are practically limited to GaAs etch rates of 1 μm/min or less. Batch loading of multiple wafers has provided a means to improve wafer throughput, but this becomes impractical as wafer size has moved from 75mm through 100mm to 150mm.

More recent work has focused on process development using chlorine-based chemistries in high density etch platforms such as inductively coupled plasma (ICP)[13-16] and electron cyclotron resonance (ECR)[17-20] reactors. While the ECR configuration is capable of higher plasma densities than an ICP, problems associated with scaling it to wafer sizes greater than 100 mm have precluded its widespread use as a high volume manufacturing solution.

In this paper we characterize a manufacturable ICP-based high rate (10 μm/min) GaAs via etch process. This work is an extension of a production qualified 6 μm/min BCl_3 / Cl_2 etch process[16]. In that work pillar-like features were observed in some fraction of the sample vias. Pillar formation was found to be a strong function of the substrate type (***Figure 1***). The present work was performed on the substrate type most prone to pillar formation (Vendor A) in an effort to develop a robust process that yields pillar-free etching independent of substrate type.

Through the use of designed experiments, the GaAs etch rate, GaAs:photoresist etch selectivity and feature profile were explored as a function of process gas composition, ICP power, RF bias power and pressure.

Experimental

All wafers were etched on a Unaxis VLR 700 GaAs Via etcher. This commercially available tool uses a 2MHz RF inductively coupled coil to generate a high density plasma. Ion energy at the wafer surface is independently controlled by a 13.56 MHz RF

bias applied to the cathode. Wafer temperature is maintained through the use of a fluid cooled cathode in conjunction with electrostatic clamping and He backside cooling. Plasma emission was monitored using a Unaxis Spectraworks optical emission spectrometer (OES). The spectral range was 200 – 800 nm with a resolution of 1 nm using a 25 μm slit. The CCD detector was coupled to the sapphire reactor viewport with a silica optical fiber.

The substrates etched in these experiments were 150 mm semi-insulating mechanical GaAs wafers patterned with a 14 μm thick photoresist mask. The total exposed area of the test pattern was approximately 15%. A large portion of the exposed area was due to a 3 mm photoresist edge bead removal process. Samples were exposed to plasma for 6 minutes unless otherwise noted.

All GaAs etch depth measurements were taken using a step profilometer (Tencor P11). Initial and post-etch resist measurements were performed using a reflectance spectrometer (Nanospec 6100). Cross sections were analyzed by optical and scanning electron microscopy.

Results and Discussion

Plasma etch processes for GaAs typically utilize a chlorine based chemistry. As would be expected for a primarily chemically driven etch process, numerous studies have shown that the GaAs etch rate increases with increasing Cl concentration. In previous studies the Cl concentration has been increased by increasing pressure, increasing the percentage

Cl_2 in the feed gas composition, increasing total flow, or some combination of these factors.

The dependence of GaAs etch rate on pressure has been widely reported – particularly in the RIE configuration. Chen et. al[20] investigated the effect of higher process pressures (up to 50 mtorr) in an ECR configuration using an Ar / Cl_2 based process. The increased etch rate (6.7 μm/min) was at the expense of feature profile control with higher pressure processes resulting in isotropic etch profiles.

Increasing the etch rate by increasing the Cl_2 fraction in the feed gas composition has also been widely reported. Shul et. al.[13] investigated ICP-based Ar / Cl_2 processes and found a maximum etch rate at a composition of 90% Cl_2. Constantine et. al.[14] investigated ICP-based BCl_3 / Cl_2 processes and found no etch rate increases for Cl_2 compositions greater than 75% Cl_2.

Increasing the total flow of process gases has also been shown to increase GaAs etch rate at a fixed process pressure. The increased flow reduces the residence time of reactants, raising the concentration of available Cl while reducing the concentration of etch byproducts. Recent work has been reported for gas flows up to 200 sccm with a maximum etch rate of 10 μm/min[21].

The present work explores the process space at ultra high gas flows (> 500 sccm) at relatively low operating pressures (< 25 mtorr) resulting in gas residence times on the

order of 0.1 seconds. Screening experiments over a range of process pressures and ICP powers confirm the relationship between process gas flow and GaAs etch rate (see ***Figure 2***). During these screening experiments a maximum anisotropic etch rate of over 15.5 μm/min for a 100 micron diameter feature was observed.

Based on the screening experiments, a designed experiment (DOE) was performed to map out the process space for high flows. While factorial experiments are a reliable way to map process responses, they quickly become cost prohibitive for a larger number of factors. Fractional factorial experiments are a convenient way to map factor responses, balancing time and material requirements with the quality of the calculated responses.

A four factor half fractional (2^{4-1}) design was chosen to explore the process window. This design explores the process space of 4 factors in only 11 experiments (8 + 3 centerpoint repeats) but is unable to resolve two factor interactions. If a two factor interaction is indicated in the statistical analysis, further experiments would be required to isolate the interaction. No significant two factor interactions were indicated during the analysis of variance for these experiments.

The designed experiment looked at four factors (pressure, ICP power, RF bias power, and feed gas composition). ***Figure 3*** shows the range over which the factors were varied along with a schematic diagram of the half fractional design. During these experiments reactor temperatures, etch times, total process gas flow and hardware configuration were held constant. Note that total flow was held at a high (525 sccm) constant value based

on the results of the screening experiment. This flow / pressure combination resulted in a 0.13 second gas residence time for the centerpoint process.

During the designed experiment, wafers with premeasured resist thicknesses were etched per the assigned recipe. Once etched, the wafers were inspected top down via optical microscope at 500x magnification to qualitatively assess the etched surface morphology. Following inspection, the final resist thickness was measured via reflectance spectrometer and the resist stripped. Following resist strip, the GaAs etch depth was measured by step profilometer. From these measurements, the GaAs etch rate, resist etch rate, and GaAs:photoresist etch selectivities were calculated. Feature profiles were evaluated by cross sectional SEM analysis. ***Figure 4*** summarizes the DOE trends.

During the analysis of the designed experiment the factor effects for each response were calculated and ranked using statistical software (Design Expert 6.0 – Stat Ease Co). A half-normal plot was constructed in order to determine which factors reside above the noise floor and should be included in the model. Once the model factors were chosen, analysis of variance calculations were performed to determine if the model was adequate to map the response over the factor space.

In the process space explored by the designed experiment, the GaAs removal rate increased solely with increasing ICP power (***Figure 5***). Previous designed experiments have shown GaAs etch rate to be a function of pressure, ICP power and feed gas

composition which is expected for a purely chemical etch mechanism. In these experiments, ICP power may be the sole factor affecting etch rate for two reasons:

- The GaAs etch rate may be limited by the fraction of the Cl_2 fed to the reactor which is dissociated into reactive Cl by the plasma. The degree of dissociation is expected to be dependent on the ICP power. The combination of high flows at low pressures yields short residence times (~ 0.1 seconds) which may result in a large excess of undissociated Cl_2.
- The DOE is limited to modeling the responses over the range of factors tested. Pressure and composition are still likely to affect the GaAs etch rate, just not significantly over the range of factors tested (9-15 mtorr & 80-90% Cl_2).

It is important to note that due to metrology considerations, the DOE results are reported on 100 μm features. Due to the chemical nature of the GaAs via etch process, there is a large dependence of etch rate on feature aspect ratio[22,23]. In an effort to quantify this relationship in the ultra-high flow regime, further validation experiments were performed using the centerpoint process. ***Figure 6*** shows the relationship between feature size and etch rate.

The argument to pursue faster GaAs etch rates is to decrease throughput time and ultimately cost of ownership. In order to realize these cost savings, etch rate alone is not sufficient. If the higher etch rate comes at the expense of poor etch rate uniformities, much of the time saved during the shorter main etch step is lost in the longer overetch times required to clear all features across the wafer. One of the benefits of etching in a

high flow, low pressure regime is the ability to achieve fast etch rates while maintaining excellent etch rate uniformity across the wafer. ***Figure 7*** shows a uniformity map measured across a 53-point, regularly spaced array of 100 micron features with a 5 mm edge exclusion. For the 10 μm/min centerpoint process the GaAs etch rate uniformity was found to be ±2.8% (Range / 2 * Mean).

The photoresist removal rate was found to be a strong function of RF bias power and ICP power and a weaker function of process pressure. The increase of resist etch rate with RF bias power and ICP power is consistent with a physical (sputtering) etch mechanism. Increasing RF bias increases the energy of ions bombarding the wafer surface while increasing ICP powers will increase the ion density, or flux, of ions bombarding the wafer surface. Both of these trends are consistent with a physical etch mechanism. The resist etch rate decreased with increasing pressure which is still consistent for a physical etch process – the rate of a chemically driven process typically increases with increasing reactant concentration (pressure).

The GaAs:Photoresist etch selectivity was determined by taking the ratio of the GaAs etch rates to the photoresist etch rates. GaAs:Photoresist etch selectivity was found to be solely a function of RF Bias power over the range of factors explored. Selectivity decreased with increasing RF Bias power. The etch selectivity can play a large role in the manufacturability of a via etch process – particularly when a sloped via profile is required. Clayton et. al.[16] discussed the relationship between etch selectivity, initial photoresist profile and the final via profile. It is important to note that selectivity (and

potentially profile) is a function of RF Bias power while the GaAs rate is not. This allows the process to be adjusted over a wide range of via profiles, from vertical to highly sloped, independent of the GaAs etch rate.

Immediately following etch (prior to resist strip) the wafers from the designed experiment were inspected optically for the presence of pillars in the vias. While most of the process conditions resulted in pillar free vias, a few design cells, particularly those at low ICP powers did exhibit some pillar formation. Attempts to model this response for the current design did not yield a model that could adequately map the response.

In an effort to quantify this response, additional experiments using "vendor A" (those substrates most prone to pillar formation) substrates were performed. While no statistically significant response was obtained between pillar formation and the factors tested (RF bias power, ICP power, pressure, and composition), graphing observed pillar counts against the GaAs:photoresist etch selectivity (***Figure 8***) shows a clear qualitative trend. Pillar formation increases as the etch selectivity decreases. This relationship highlights the potential tradeoff between achieving sloped profiles while maintaining pillar-free vias – particularly for "vendor A" substrates. This result contradicts the previous work of Nam et. al.[24] who found that pillar formation was reduced at higher RF bias powers. This apparent contradiction may be a result of the different process regimes explored in the two studies (2.8 μm/min @ 60 sccm total flow vs. 10 μm/min @ 525 sccm total flow for current work).

Following the analysis of the individual responses, a map of the process space was constructed (see ***Figure 9***) constraining the GaAs etch rate to greater than 10 μm/min with a GaAs:Photoresist etch selectivity greater than 13:1 to ensure a sloped via using a sloped resist mask.

Based on the preceding experiments, additional mechanical wafers were etched to validate process conditions aimed at providing a high rate (10 μm/min) via etch process with a sloped feature profile that minimized pillar formation. ***Figure 10*** summarizes the etch results along with an optical cross section of a typical 40 μm diameter via.

Conclusions

In this article we report a high rate GaAs via etch process using a BCl_3 / Cl_2 based chemistry in a commercially available ICP reactor. GaAs etch rates in excess of 15 μm/min were reported for a near room temperature process using ultra high gas flows (greater than 500 sccm) at relatively low pressures (less than 20 mtorr). This process regime results in process gas residence times on the order of 0.1 seconds ensuring a high concentration of reactive Cl at the wafer surface. During the course of these experiments, pillar formation was observed in a limited number of design cells. Additional experiments showed that pillar formation increases as the GaAs:photoresist selectivity decreases. This relationship highlights the potential trade-off between eliminating pillar formation and the amount of slope achieved through erosion of a sloped photoresist mask

Through the use of designed experiments a production worthy GaAs-via etch process was characterized. This process is capable of fast etch rates (10 μm/min @ 100 μm diameter, 8.3 μm/min @ 40 μm diameter) over a wide range of GaAs:photoresist etch selectivities. Over the range of parameters explored, the RF Bias power allowed independent control of the GaAs:photoresist etch selectivity and ultimately via profile with the use of a sloped photoresist mask.

Acknowledgments

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Figure Captions

Figure 1. Pillar formation as a function of substrate supplier. Material D shows 80% pillar free vias on thinned and mounted 150mm GaAs slices. Material A shows 10% pillar free vias for the same process conditions. [16]

Figure 2. Effect of Cl_2 flow rate on GaAs etch rate. Graph summarizes a number of screening experiments performed over a range of pressures, feed gas compositions and ICP powers.

Figure 3. Summary of designed experiment. Range of factors explored and schematic of 2^{4-1} design. Black nodes on design schematic indicate experimental conditions.

Figure 4. Response trends from designed experiment.

Figure 5. Analyzed GaAs etch rate response from designed experiment. A. Half normal plot showing ICP power as the only significant factor affecting GaAs etch rate over the range of parameters tested. B. Factor effect plot showing GaAs etch rate as a function ICP power.

Figure 6. GaAs etch rate as a function of feature width. Etch rates determined from multiple cross sections of a single wafer etched at the DOE centerpoint process for 6 minutes. Multiple sizes of vias and trenches were sampled.

Figure 7. GaAs etch depth uniformity from the DOE center point process. The uniformity map was constructed from a 53-point regularly spaced array using a 5 mm edge exclusion. The wafer was etched for 6 minutes.

Figure 8. Pillar count as a function of GaAs:photoresist etch selectivity (substrate "vendor" A material). Note the potential trade-off between pillar formation and final via etch profile.

Figure 9. Process space as a function of ICP power and RF bias power.

Figure 10. Summary of process capability for optimized GaAs via etch process. Inset micrograph shows optical cross section of 40 μm diameter via – note slope induced by erosion of sloped photoresist mask.

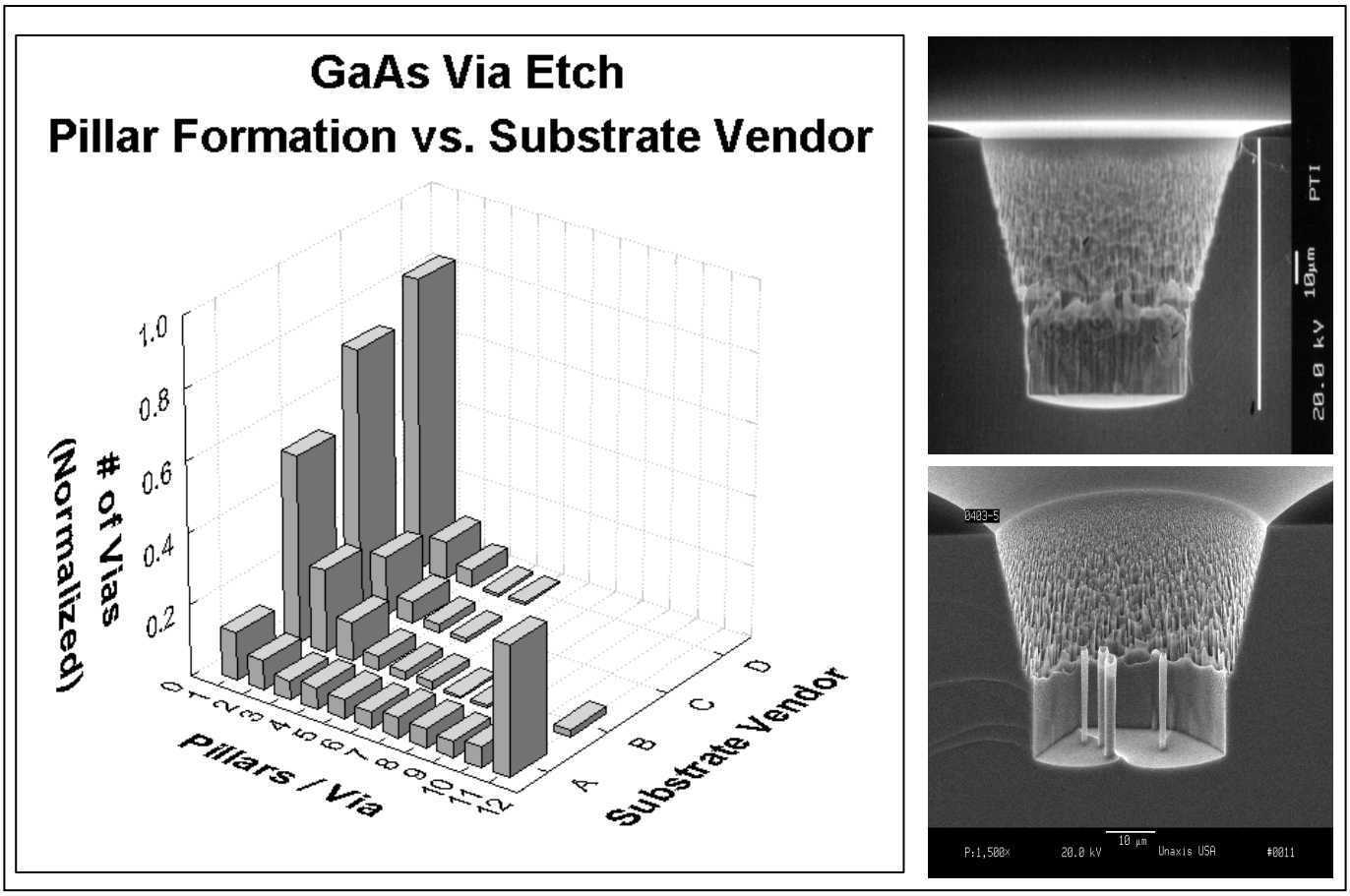

GaAs Via Etch
Pillar Formation vs. Substrate Vendor
# of Vias (Normalized)
1.0
0.8
0.6
0.4
0.2
Pillars / Via
Substrate Vendor
A
B
C
D
20.0 kV 10µm PTI
0403-5
10 µm
P:1,500x
20.0 kV
Unaxis USA
#0011

Figure 1.

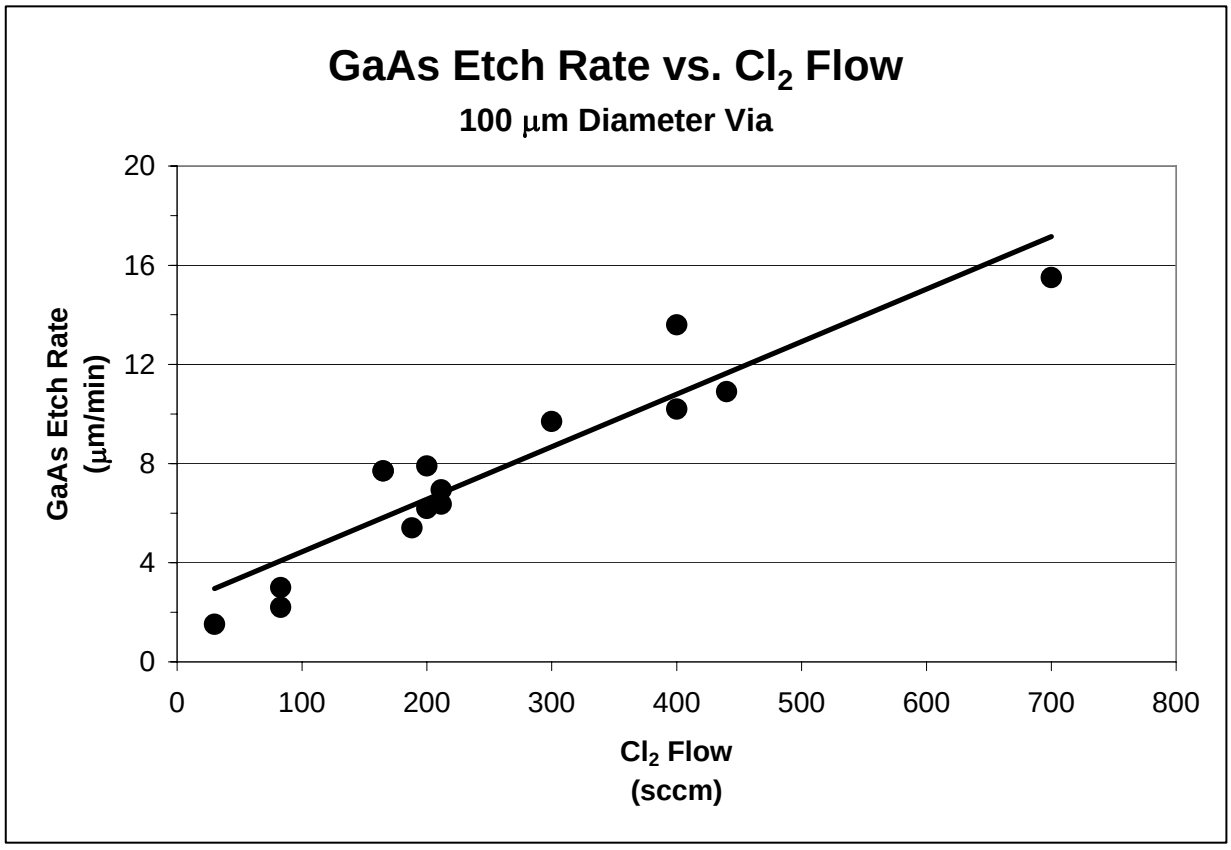

GaAs Etch Rate vs. Cl2 Flow
100 μm Diameter Via
GaAs Etch Rate (μm/min)
0
4
8
12
16
20
0
100
200
300
400
500
600
700
800
Cl2 Flow (sccm)

Figure 2

Design Layout

Factor Name		Low	High
Pressure	mtorr	9	15
ICP	W	800	1400
RIE	W	135	155
% Cl_2	%	80	90

Constants

Total Flow	525 sccm
Etch Time	5 min
Temperature	15 C
Hardware	GaAs Via III

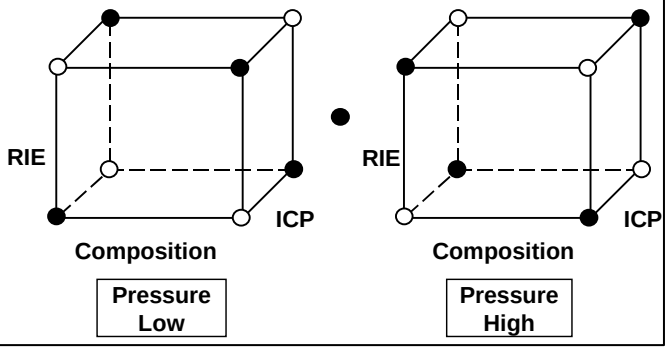


Figure 3

	Response	Response			
Factor		GaAs Rate	Resist Rate	GaAs:Resist Selectivity	DC Bias
	↑ Pressure		↓		↑
	↑ ICP	↑↑	↑↑		↓↓
	↑ RF Bias		↑↑	↓↓	↑↑
	↑ % Cl_2				

Figure 4

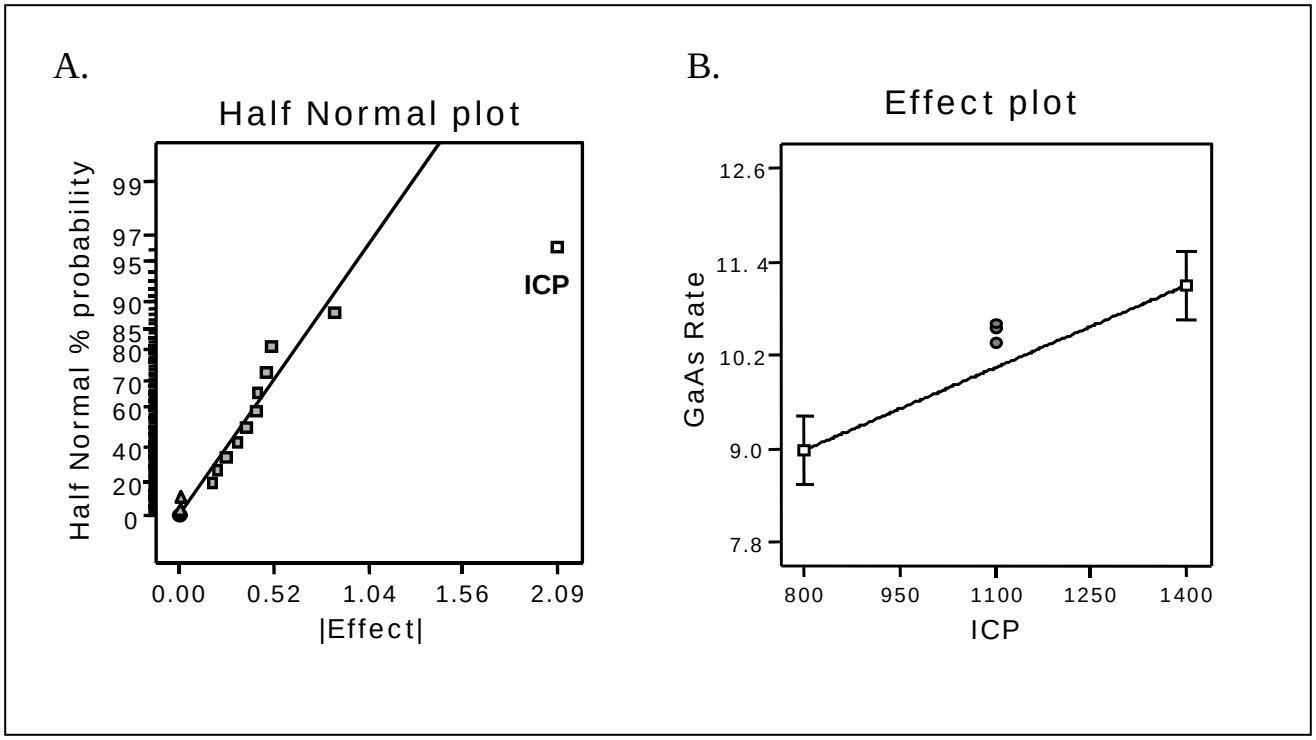

A.
Half Normal plot
Half Normal % probability
99
97
95
90
85
80
70
60
40
20
0
ICP
0.00
0.52
1.04
1.56
2.09
|Effect|
B.
Effect plot
GaAs Rate
12.6
11. 4
10.2
9.0
7.8
800
950
1100
1250
1400
ICP

Figure 5

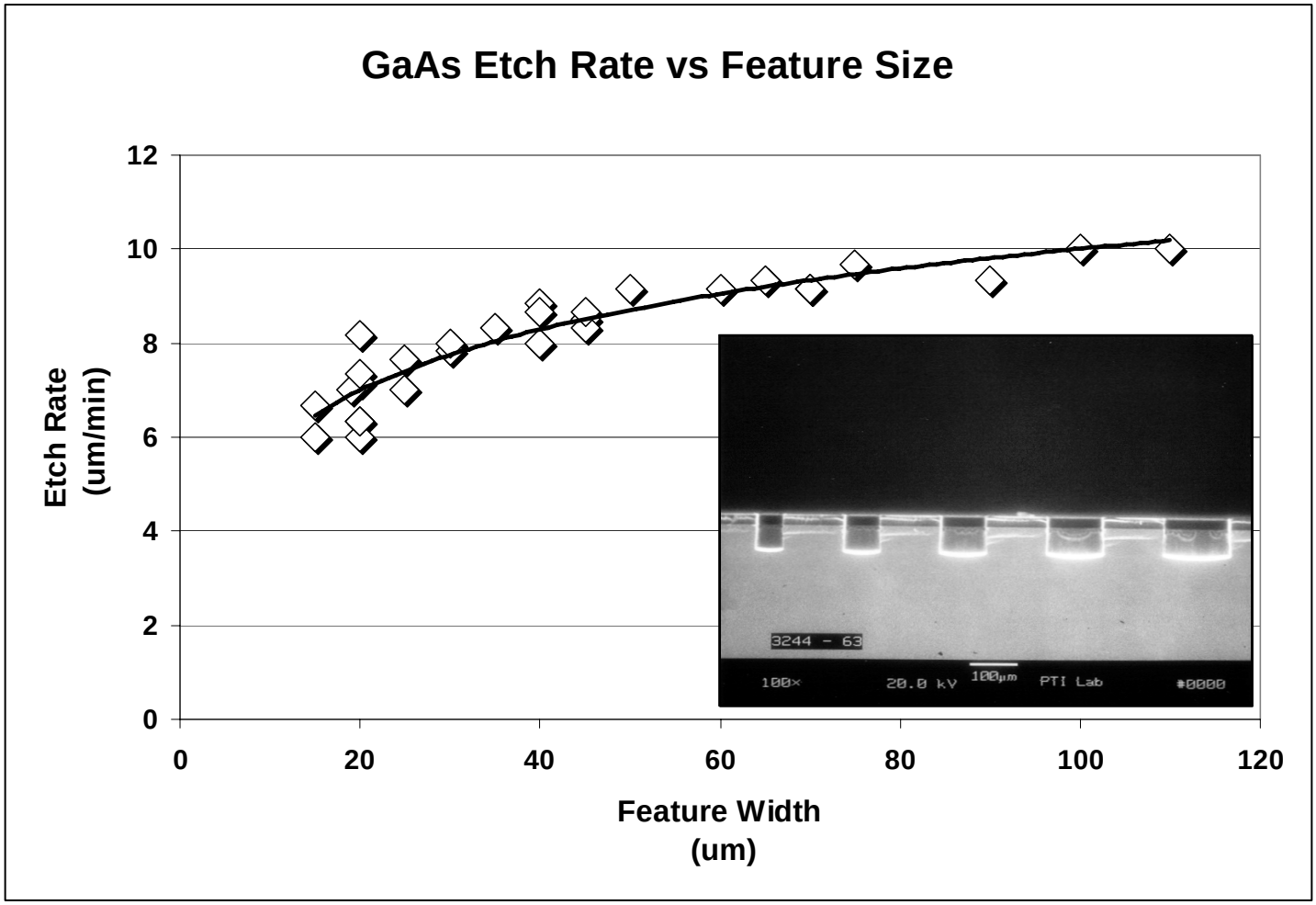

GaAs Etch Rate vs Feature Size
Etch Rate (um/min)
0
2
4
6
8
10
12
0
20
40
60
80
100
120
Feature Width (um)
3244 - 63
100×
20.0 kV
100µm
PTI Lab
#0000

Figure 6

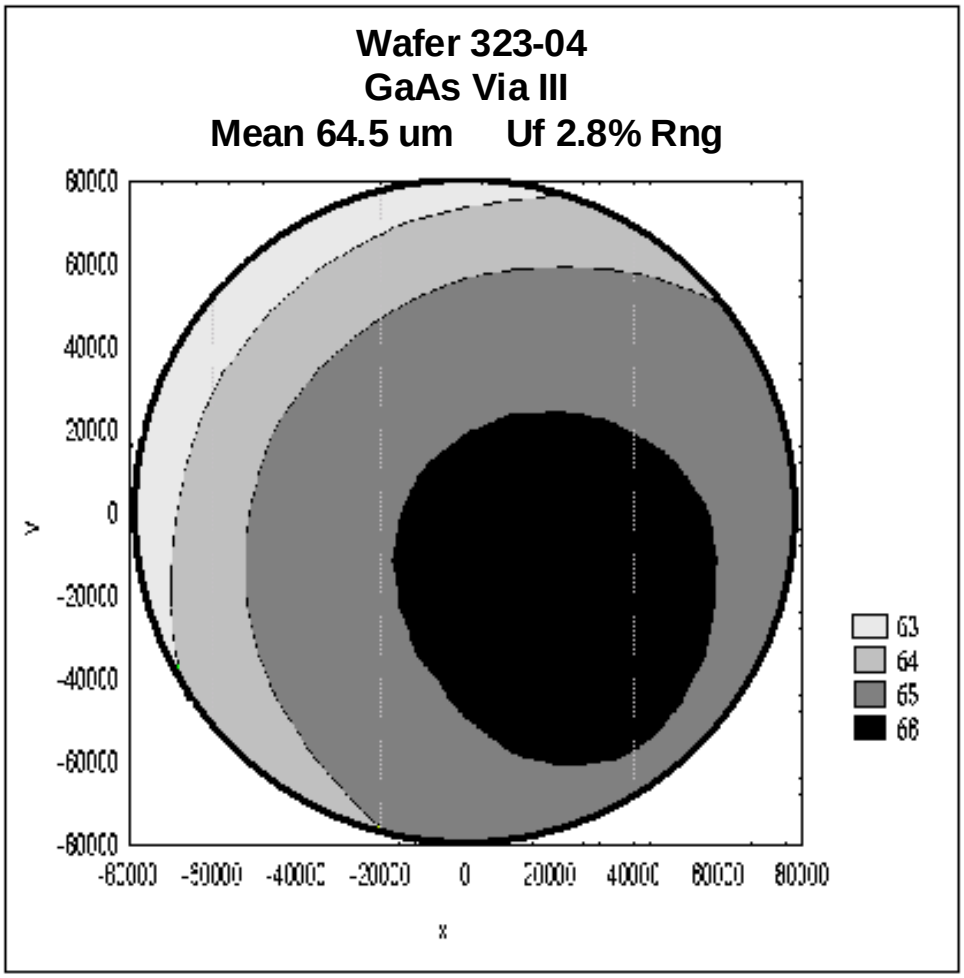

Wafer 323-04
GaAs Via III
Mean 64.5 um Uf 2.8% Rng
60000
40000
20000
0
-20000
-40000
-60000
-80000
y
-80000
-60000
-40000
-20000
0
20000
40000
60000
80000
x
63
64
65
66

Figure 7

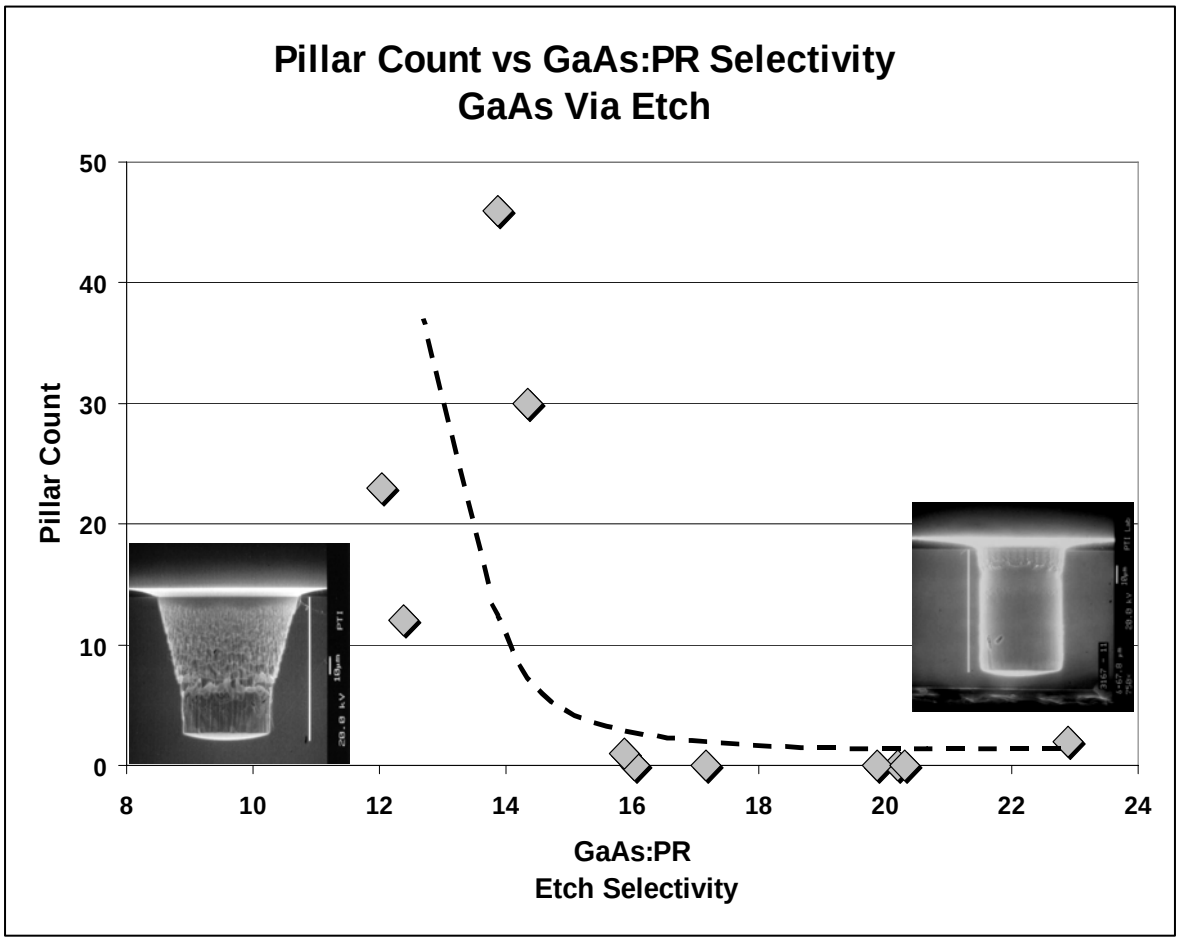

Pillar Count vs GaAs:PR Selectivity
GaAs Via Etch
Pillar Count
50
40
30
20
10
0
8
10
12
14
16
18
20
22
24
GaAs:PR
Etch Selectivity

Figure 8

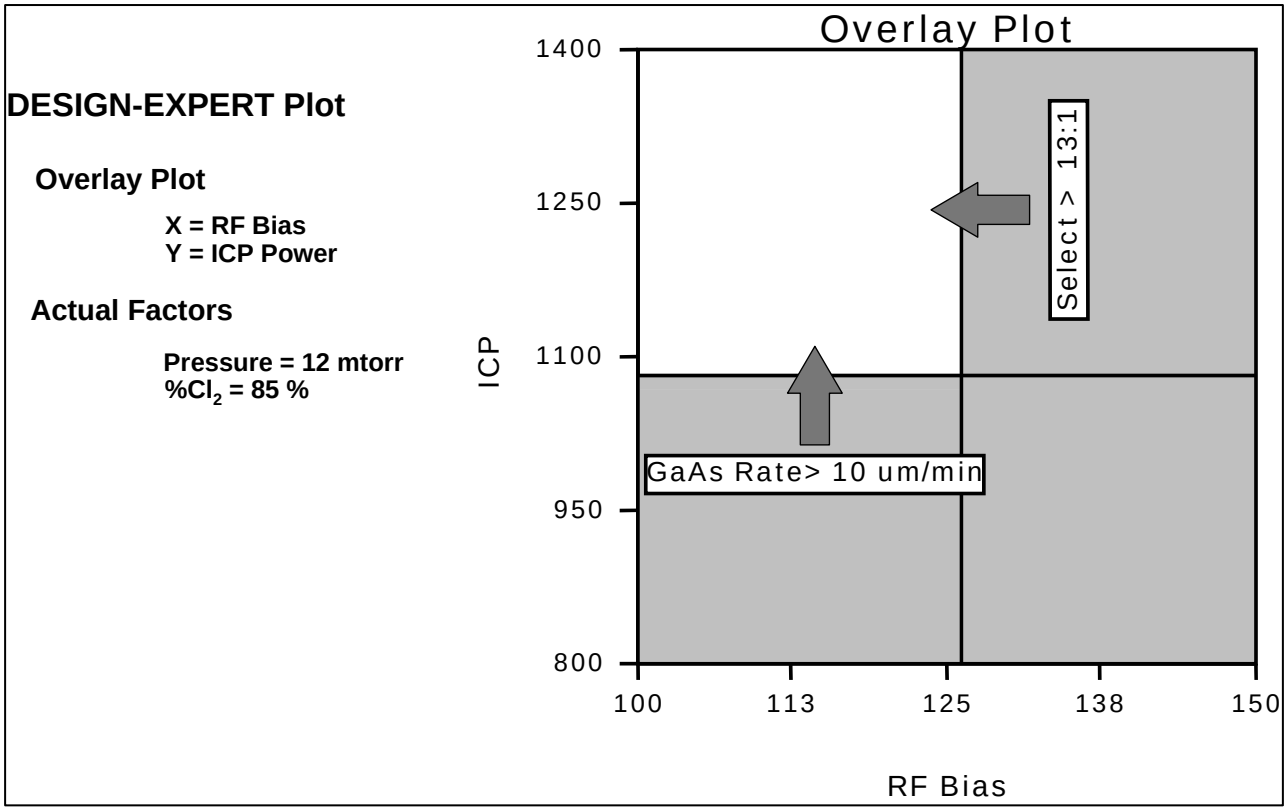
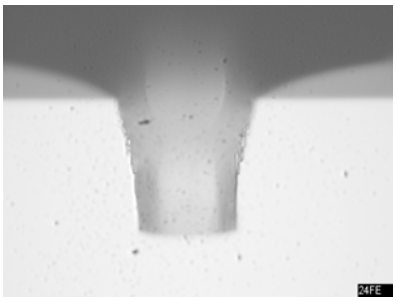

DESIGN-EXPERT Plot
Overlay Plot
X = RF Bias
Y = ICP Power
Actual Factors
Pressure = 12 mtorr
%Cl2 = 85 %
Overlay Plot
1400
1250
1100
950
800
ICP
Select > 13:1
GaAs Rate> 10 um/min
100
113
125
138
150
RF Bias

Figure 9

GaAs Via III - Process Performance

GaAs Etch Rate	**8.3 um/min – 40 um via** **10.1 um/min – 100 um via**
GaAs:PR Selectivity	**15 : 1**
Via Profile	**Sloped ***
GaAs Rate Uniformity	**< 5%**
Morphology	**Specular**



Optical cross-section of 40 um diameter via

***** using sloped PR mask

Figure 10.