Photomask SBU: 65nm Dry Etch has Arrived!

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What's New in Lithography?

Wafer dimensions are still accelerating downward towards ever smaller features and the legendary Moore's Law is still valid for current silicon devices. As wafer IC dimensions approach the physical limitations of silicon physics, the lithography techniques used to print these patterns on Silicon become very difficult to perform.

Current Wafer Scanners are able to print 90 nm Technology Node features with new 193 nm wavelength light sources. In fact, recent trends clearly show that 65nm Technology Node features will be possible with these Scanners. Some in our industry believe that novel optical adjustments to Wafer Scanners (i.e. water immersion lenses) will allow this technology to extend even to 45 nm feature sizes!

Through all this, the venerable Photomask is expected to remain the primary transfer medium ~~Master Stencil of the~~ for mass producing integrated circuit patterns. ~~and~~ Of course, wafer lithography now requires the use of newer Photomask techniques such as Phase Shift Masks in order to achieve the very small features demanded by the current International Technology Roadmap for Semiconductors (ITRS).

Now, more than ever before, etching Binary Chromium (Cr) Masks is the resolution-limiting step within the manufacturing process of advanced Masks Sets. Again, our industry has worked hard to surpass the current ITRS Roadmap. We've brought the 65nm Technology Node within reach more than one year earlier than predicted; we expect 90 nm Node Technology Masks to be prototyped within Q4 2003 and 65nm Node Technology Masks to be prototyped Q3 2004. This is fully 12 months earlier than the most recent Roadmap ,which was itself, considered quite aggressive in 2002!

Here Comes 65nm!

For more than 12 months, the Unaxis Photomask SBU has been developing new etch technology focused on the 90nm and 65nm Technology Nodes; we believe this fourth generation (***Gen 4)*** ICP system is quite unique and will again allow our customers to push the limits of optical lithography. Gen 4 etch equipment will be mandatory for the Photomask Industry for a number of reasons:

Mask Error Budget: Three major manufacturing technologies are utilized in the production of photomasks:

1. Pattern Generation: Writing (or exposure) of the circuit pattern information into a photo-sensitive resist on the mask blank.
2. Resist Develop: Wet chemical removal of resist in the exposed pattern areas on the mask blank.
3. Absorber Etch: Wet chemical or ICP dry etch of the photo-absorber material (Cr, MoSi, etc.) using the developed resist as an etch mask.

Each of these manufacturing processes contributes a portion of error to the formation of the actual vs. ideal pattern information. Any pattern deviation is typically known as the mean-to-target error, where "target" describes the various feature sizes and feature placement of the circuit pattern as originally designed on the computer. The "mean" aspect describes how the manufacturing process(es) altered those features and their placement on the final mask. Obviously, as features sizes have continued to shrink, the allowable "mean-to-target" error budget has had to shrink proportionately. This has posed a significant problem in general for all mask

manufacturing processes, but has posed a particularly difficult problem for the mask etch process as follows:

1. Pattern Generation: The accuracy of exposure tools has improved significantly over the past 5-10 years with smaller grid and beam sizes, enabling these tools to describe ever smaller features in the resist and place those features in more closely controlled proximity. However, resist systems have not evolved in concert with the beam placement accuracy of the pattern generators. In recent years, important advances in resist chemistry have been in the form of "fast" resists which can be exposed with low beam energy (e.g. Chemically Amplified Resists). But, almost no advancement has occurred in resist materials as it pertains to final image formation, resist thickness, feature sidewall angle, residue, material stability, etc. (all things that would make the etch step easier). The net result is, pattern generator accuracy has improved substantially with regard to placement and overlay accuracy, but for overall feature fidelity (CD uniformity, feature resolution, feature size linearity, etc.), the pattern generators cannot fully absorb their fair share of the smaller error budget needed for the 90nm Technology Node. And with no new resist systems in sight, they cannot be expected to absorb any further error budget as we move into 65nm Technology Node mask making.

2. Resist Develop: The minimal evolution of resist systems equates literally to zero advancement in the method and accuracy of the resist develop. This process step has not and will not be able to absorb any additional reduction in error budget.

3. Cr Etch: It should now be painfully clear that the only manufacturing step left to absorb the ever smaller error budget needed to meet the 90nm and 65nm mask making challenge is the etch process. One of the foremost advances in absorber etch technology came from Unaxis in 1995 with the introduction of ICP dry etch technology. Since that time, Unaxis has introduced three successive generations of improved dry etch systems. Now the collapsing ITRS roadmap has forced us once again to reduce the error tolerances in our equipment technology (enter Gen 4).

Figure 1. illustrates the evolution of dry etch error budgets required for key performance parameters at the various technology nodes over the past eight years (Gen 1-3) and the error budget requirement today and in the near future (Gen 4).

Mask Dry Etch - Key Performance Specifications

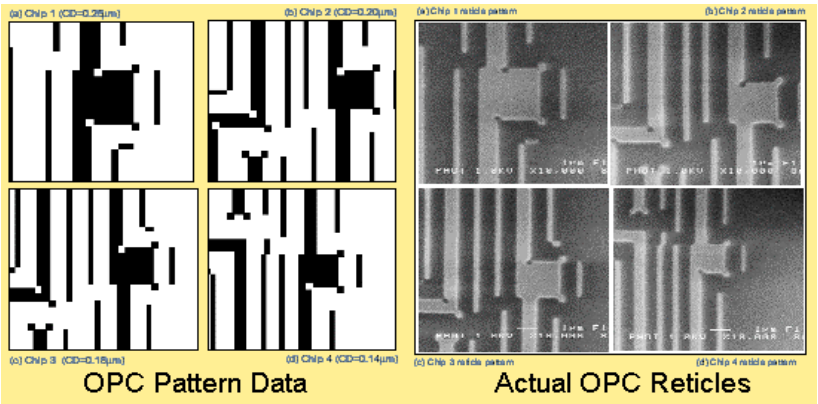
Year	Unaxis Model No. (Technology Node)	CD Uniformity (3 sigma)	CD Linearity (Range)	Etch Bias (Average)
1995	Mask Etcher I (0.18µ)	35nm	- N/A -	- N/A -
1998	Mask Etcher II (0.15µ)	25nm	- N/A -	80nm
2001	Mask Etcher III (0.13µ)	15nm	20nm	45nm
2003	Mask Etcher IV (90nm)	8nm	15nm	30nm
2004	Mask Etcher IV (65nm)	6nm	8nm	20nm

Figure 1.

Dramatic performance improvements in dry etch system technology have been needed and achieved by Unaxis during the past eight years to keep the mask industry in step with the lithography demands of the device designers. So far, we are on-track to continue this dry etch performance improvement trend.

Feature Size Resolution: Wafer IC dimensions are becoming so minute, they are literally smaller than the wavelength of the stepper light used to expose them on the wafer. As discussed earlier, one method of overcoming this problem is the use of special mask materials that provide half-wave attenuation or "phase shifting" of the Stepper light; this produces exposures on the wafer even smaller than the exposure light wavelength. Another, more common method of resolving features on the wafer is to employ what are called "Optical Proximity Correction" (OPC) features on the photomask. These are printed features on the mask that are too small to resolve at the wafer level, but they do add light to the edges and corners of very small features on the wafer. This "light assist" technique has been used effectively by pattern designers for many years.

Advanced Device Patterning Requires Very High Resolution Imaging: e.g. Optical Proximity Correction (OPC)



OPC Serifs on the Photomask add light at the edges and corners of a feature when printed on the wafer

Figure 2.

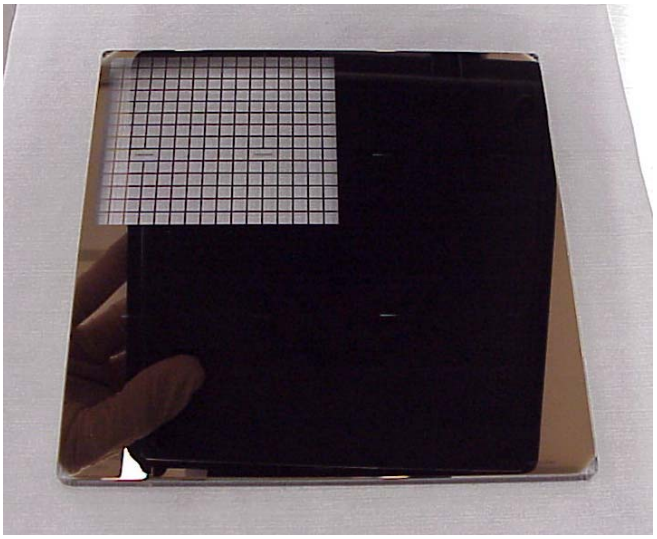
What has become problematic for mask makers is that as average feature size dimensions decrease, OPC feature sizes on the mask are becoming too small to resolve. Figure 2. illustrates typical OPC features on an advanced photomask for a 0.13µ Technology Node device. Some of the OPC features shown are less than 200nm wide. As we move to the 65nm Technology Node, OPC features will shrink to less than 100nm. Very high resolution dry etch is the only answer.

Feature Size Linearity: Another challenge facing the photomask industry as geometry's diminish is the variety of small to large features on the same pattern level that must be precisely sized. For Technology Nodes ≥0.15µ, the average mask level would typically have only one primary feature that needed to be sized as closely as possible to the original circuit design parameter. All other features on that mask level, smaller or larger than the primary feature, could be slightly under or over-sized because their dimensions were relatively inconsequential to the final device performance. This is no longer the case at 90nm. For example, on a 90nm mask, the primary design feature together with its various OPC features must all be sized as close as possible to their original design criteria because the margin for error on the wafer is so small. Figure 1. corroborates this new challenge. Note that in 1998, at the 0.15µ Technology Node, CD Linearity was not even a specified performance parameter. But, by 2001, CD Linearity appears as a mask etcher performance requirement at less than half the total etch bias. Also note, this requirement continues to drop dramatically with each new Technology Node.

Bright Field/Dark Field Linearity: Mask Etcher III® was an enormous breakthrough for the mask industry. This Gen 3 system was able to optimize the plasma etch of Chromium films on glass so that the uniformity for high load Cr patterns and low load Cr patterns are the same. This was a major step forward for the industry and provided a large yield improvement for most masks shops. This was, of course, during a time when most device pattern layers were fairly uniform

across each mask, creating evenly distributed high or low Chrome loads on different masks. However, as device geometry's have grown smaller, device designs have grown more sophisticated. Logic devices now have large imbedded memory cells. Memory devices now have on-board logic circuits. The net result of all this circuit integration are patterns with large open cells on the same layer, creating masks with large areas of unevenly loaded Chrome. In other words, mask makers are now faced with high and low Chrome loads on the same mask.

Unaxis "Ybor" (1-window) Test Mask



Highly uneven pattern with >99% Cr load in window and <1% Cr load on remaining area.

Figure 3.

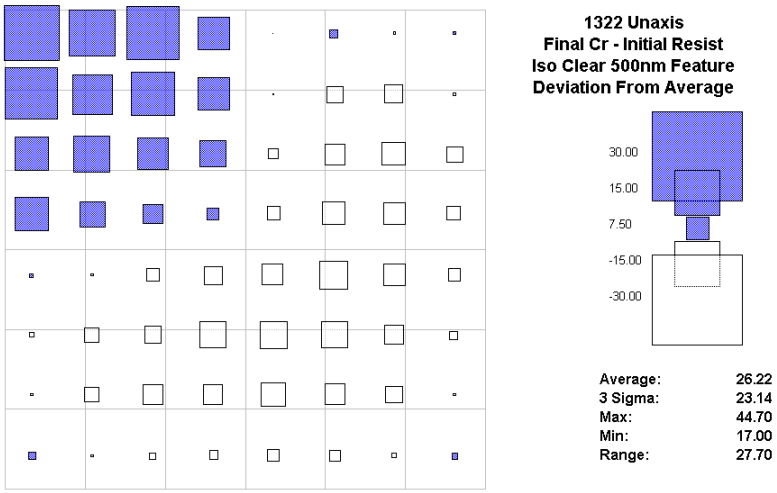
Figure 3. is a picture of the "Ybor" Unaxis dry etch test mask used to emulate the high/low Chrome load conditions of an advanced mask layer. The test features are written in FEP171 Chemically Amplified (E-Beam) Resist. There are 64 measurement sites covering a 135mm x 135mm patterned area. Each site contains a variety of iso/dense and clear/dark features. This kind of pattern layer is a mask maker's bad dream and is aptly named a "Nightmare" mask level by the industry at large. As device designs evolve, mask makers are seeing more and more of these advanced "Nightmare" mask levels.

The desired etch for this type of mask layer is to achieve a very low total etch bias in both the clear field (window) and the dark field (low Cr load area) while at the same time producing a very low Critical Dimension (CD) Uniformity for the full range of feature sizes (Feature Size Linearity). And by the way, do all this while keeping the Cr profile as close to 90° as possible.

Why Gen 4?

Until now, the required dry etch process improvement has not been forthcoming to support the performance level needed for 90nm lithography. Over the past two years, the Unaxis Gen 3 ICP source has proven itself to be the most advanced dry etch reactor technology in the market; superior in all performance categories to any other competitive tool. But, as good as it is, even our Gen 3 ICP reactor has trouble dealing with this asymmetrically loaded etch challenge.

Ybor (1 window) Test Mask - Gen 3 Etch Signature



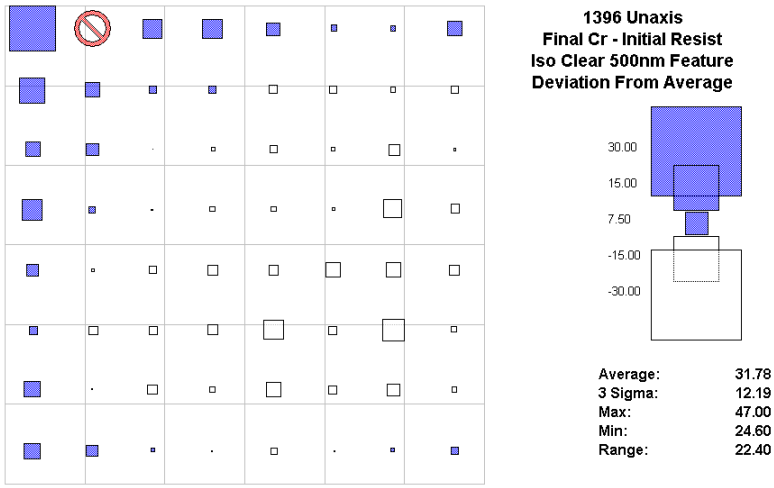
Best "Gen 3" dry etch process shows very large Brightfield/Darkfield etch signature disparity in the clear (window) vs. the dark (outer) area.

Figure 4.

Figure 4. is a box plot that gives a pictorial representation of the dry etch contribution across an Ybor (1 window) test mask (# 1322) using a Unaxis Gen 3 ICP source. The various box sizes illustrate the relative CD Uniformity (of 0.5µ features) across the mask based on the amount of under or over etch of each feature from the average etch bias. Note that the average etch bias appears quite good (26.22 nm) but the global CD Uniformity is quite high (23.14 nm, 3σ). After more than two years of process development, the dramatic Chrome load distribution on this type of mask level continues to pose a severe CD Uniformity problem for Gen 3.

More than eighteen months ago, we understood some very fundamental concepts need to be realized and a new etcher, **Gen 4**, needed to be developed in order to achieve the necessary performance improvements for 65nm mask making. Utilizing a unique and very advanced plasma ICP concept (patent pending by Unaxis), even early Gen 4 results demonstrated Resist Selectivity 2-3x normal process conditions. Furthermore, Gen 4 incorporates a vastly improved vacuum system and utilizes a radically new RF Generator arrangement that allows us to explore process areas which were not possible in Gen 3. The proof of course, is in the process performance results.

Ybor (1 window) Test Mask - Gen 4 Etch Signature



Initial "Gen 4" dry etch process shows almost no Brightfield/Darkfield etch signature disparity in the clear (window) vs. the dark (outer) area.

Figure 5.

Figure 5. is a box plot of the dry etch contribution across an Ybor (1 window) test mask (# 1396) using a Gen 4 ICP source. The first, most obvious thing to note, is the absence of the telltale etch disparity signature in the window area. The average etch bias is still quite good (31.78 nm) but, the real excitement is the global CD Uniformity, now almost half (12.19 nm, 3σ) what was typical for Gen 3.

Ybor (1 window) Test Mask - Gen 3 vs. Gen 4
Dry Etch Data Comparison Sumary

MEASUREMENT FEATURE SIZE	GEN 3 ETCH RESULTS Ybor (1 window) Test Mask # 1322	GEN 4 ETCH RESULTS Ybor (1 window) Test Mask # 1396
300nm - Iso Clear		
CD Uniformity (3σ)	23.1 nm	11.1 nm
CD Bias (Ave.)	22.4 nm	29.6 nm
500nm - Iso Clear		
CD Uniformity (3σ)	23.1 nm	12.2 nm
CD Bias (Ave.)	26.2 nm	31.8 nm
1500nm - Iso Clear		
CD Uniformity (3σ)	27.6 nm	16.6 nm
CD Bias (Ave.)	34.5 nm	29.3 nm

Dry Etch - Feature Size Linearity (Range): Gen 3 = 12 nm
Gen 4 = 3 nm

Figure 6.

Figure 6. is a more complete summary comparison of results for the two Ybor test masks #1322 and #1396. The summary includes measurement data for 300nm, 500nm and 1500nm features

across each mask. In each case, the CD uniformity from the Gen 4 etch is vastly superior to the Gen 3 results. Also note, the total Feature Size Linearity is ~3nm (Range) across the various feature sizes for the Gen 4 etch results; this is a 4x improvement over the Gen 3 etch results. High performance such as this on this advanced Mask represents a true breakthrough and literally marks a new era in dry etch technology for mask making.

We are happy to report that our new Gen 4 based system products are now a reality. The Gen 4 Alpha system has been fully operational in our applications laboratory for over two months and is busy doing process development and sample demonstrations for all customers. The first Beta Gen 4 Process Module is scheduled to ship to our Beta partner/customer. Unaxis is planning to announce the production version Mask Etcher IV® as our new flagship product at the upcoming Semicon West 2003 trade exposition on July 14, 2003.

As our latest advertisements proclaim, "65nm Dry Etch has Arrived!"