Photomask Cr Process: 65nm Plasma Etch has Arrived!

What's New in CMOS Lithography?
Wafer dimensions are still accelerating downward towards ever smaller features and the legendary Moore's Law is still valid for current silicon devices. As wafer IC dimensions approach the physical limitations of silicon physics, the lithography techniques used to print these patterns on Silicon wafers is becoming very difficult to perform.

Current Wafer Scanners are able to print 90 nm Technology Node features onto Silicon Wafers with new 193 nm wavelength light sources. In fact, recent trends clearly show that 65nm Technology Node features will be possible with these Scanners. Some in our industry believe that novel optical adjustments to Wafer Scanners (i.e. water immersion lenses) will allow this technology to extend even to 45 nm feature sizes!

As before, etching Binary Chromium (Cr) Masks (the "perfect" Master Stencil pattern) is the resolution-limiting step within the manufacturing process of advanced Masks Sets. The 65nm Technology Node is within reach almost two years earlier than predicted; we expect 90 nm Node Technology Masks to be prototyped within Q4 2003 and 65nm Node Technology Masks to be prototyped Q3 2004. This is fully 20 months earlier than the most recent Roadmap , which was itself, considered quite aggressive in 2002!

Here Comes 65nm!

Cr Etch: The ever smaller error budget needed to meet the 90nm and 65nm mask making challenge has become the responsibility of the etch process. One of the foremost advances in absorber etch technology came from Unaxis in 1995 with the introduction of ICP dry etch technology. Since that time, Unaxis has introduced three successive generations of improved dry etch systems. For more than 18 months, the Unaxis Photomask Etch Group has been developing new etch technology focused on the 90nm and 65nm Technology Nodes; we believe this fourth generation (Gen 4) ICP etch system is quite unique and will again allow our customers to push the limits of optical lithography. Gen 4 etch equipment will become mandatory for the Photomask Industry in the near future.

Figure 1. illustrates the evolution of dry etch error budgets required for key performance parameters at the various technology nodes over the past eight years (Gen 1-3) and the error budget requirement today and in the near future (Gen 4).

Mask Dry Etch - Key Performance Specifications

Year	Unaxis Model No. (Technology Node)	CD Uniformity (3 sigma)	CD Linearity (Range)	Etch Bias (Average)
1995	Mask Etcher I (0.18µ)	35nm	- N/A -	- N/A -
1998	Mask Etcher II (0.15µ)	25nm	- N/A -	80nm
2001	Mask Etcher III (0.13µ)	15nm	20nm	45nm
2003	Mask Etcher IV (90nm)	8nm	15nm	30nm
2004	Mask Etcher IV (65nm)	6nm	8nm	20nm

Feature Size Resolution: Wafer IC dimensions are becoming so minute, they are literally smaller than the wavelength of the stepper light used to expose them on the wafer. As discussed earlier, one method of overcoming this problem is the use of special mask materials that provide half-wave attenuation or "phase shifting" of the Stepper light; this produces exposures on the wafer even smaller than the exposure light wavelength. Another, more common method of resolving features on the wafer is to employ what are called "Optical Proximity Correction" (OPC) features on the photomask. These are printed features on the mask that are too small to resolve at the wafer level, but they do add light to the edges and corners of very small features on the wafer. This "light assist" technique has been used effectively by pattern designers for many years.

What has become problematic for mask makers is that as average feature size dimensions decrease, OPC feature sizes on the
e mask are becoming too small to resolve.

Feature Size Linearity: A major challenge facing the photomask industry as geometry's shrink is the variety of small to large features on the same pattern level .. For example, on a 90nm mask, the primary design feature together with its various support features must all be sized as close as possible to their original design criteria because the margin for error on the wafer is so small. Figure 1 demonstrates this trend. Note that in 1998, CD Linearity was not even a specified performance parameter. But, by 2001 CD Linearity appears as a mask etcher performance requirement at less than half the total etch bias.

Ybor (1 window) Test Mask - Gen 3 vs. Gen 4
Dry Etch Data Comparison Sumary

MEASUREMENT FEATURE SIZE	GEN 3 ETCH RESULTS Ybor (1 window) Test Mask # 1322	GEN 4 ETCH RESULTS Ybor (1 window) Test Mask # 1396
300nm - Iso Clear		
CD Uniformity (3σ)	23.1 nm	11.1 nm
CD Bias (Ave.)	22.4 nm	29.6 nm
500nm - Iso Clear		
CD Uniformity (3σ)	23.1 nm	12.2 nm
CD Bias (Ave.)	26.2 nm	31.8 nm
1500nm - Iso Clear		
CD Uniformity (3σ)	27.6 nm	16.6 nm
CD Bias (Ave.)	34.5 nm	29.3 nm

Dry Etch - Feature Size Linearity (Range): Gen 3 = 12 nm
Gen 4 = 3 nm

Figure 2 is a more complete summary comparison of results . The summary includes measurement data for 300nm, 500nm and 1500nm features across each mask. In each case, the CD uniformity from the Gen 4 etch is vastly superior to the Gen 3 results. Also note, the total Feature Size Linearity is ~3nm (Range) across the various feature sizes for the Gen 4 etch results; this is a 4x improvement over the Gen 3 etch results. High performance such as this on this advanced Mask represents a true breakthrough and literally marks a new era in dry etch technology for mask making.